Josephson-CMOS Hybrid Session

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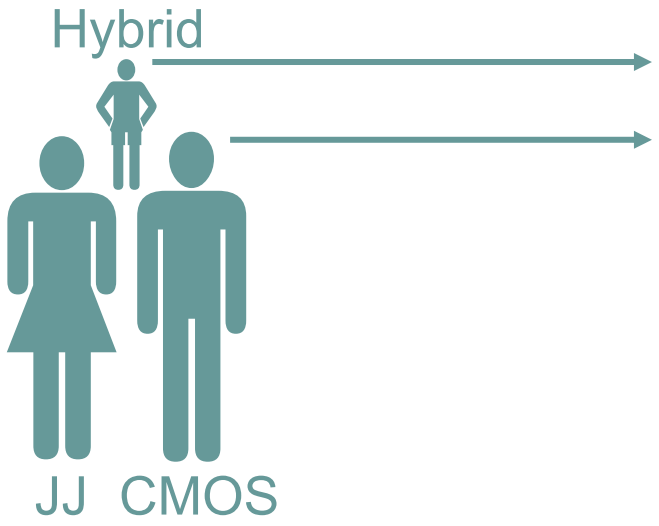
Overview

- Can we use JJs and semiconductors to make a hybrid chip or module with more performance than is available in any other way?
  - Novel hybrid circuits overview and example (Erik DeBenedictis)
- Talks on applications and benefits
  - Supercomputer with JJ processor CMOS memory (Whiteley/power)
  - AI machine with JJ neurons and CMOS support (Segall/nuc. reactors)
  - Merging Semiconductor Memory with Superconducting Logic (Razm-khah/architecture for high-performance cryogenic computing systems)
- Panel and Q&A
  - 5 min Quantum computer control (SeeQC) (Mukhanov/hard problems)
  - 5 min introductions for Jamil Kawa and Nobuyuki Yoshikawa
  - Q&A with all speakers

Standing on the Shoulders of Giants

- JJs are a giant
  - JJ: ~770 GHz toggle frequency
  - Extremely energy efficient
- CMOS
  - III-V GaAs transistors: have gain at slightly over 1 THz
  - Extremely dense
- Both giants

- Standing on the shoulders of giants allows higher speed, throughput, # of qubits/neurons, etc.



What is a Hybrid?

- “Transparent hybrid”
  - Support circuits with both JJs and semiconductor components
  - Create schematics with components and lines/wires

- Current method
  - Support systems with both JJs and semiconductors
  - All signal paths between super- and semiconductors have a transmission line or a low-pass filter

What is a Hybrid?

- Universal hybrid
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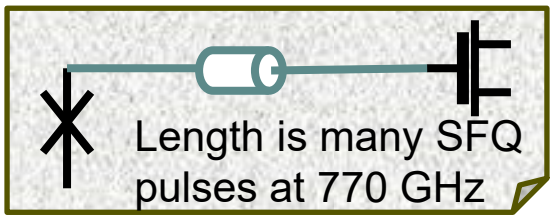

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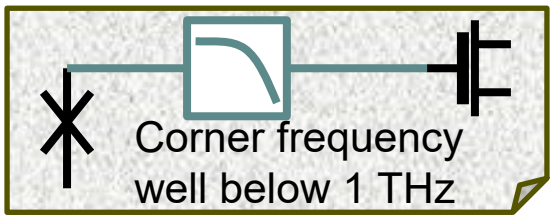
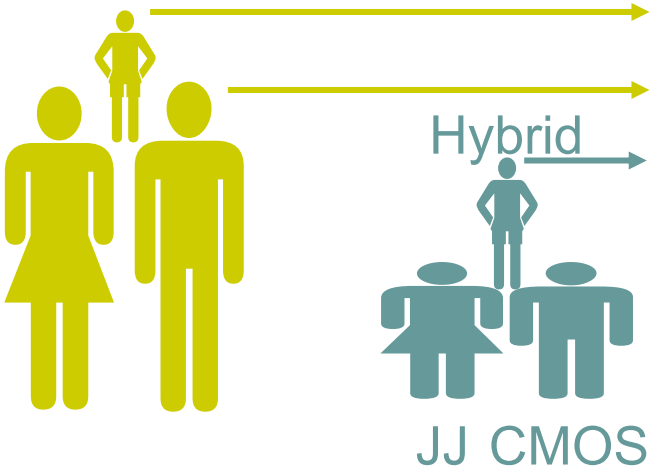
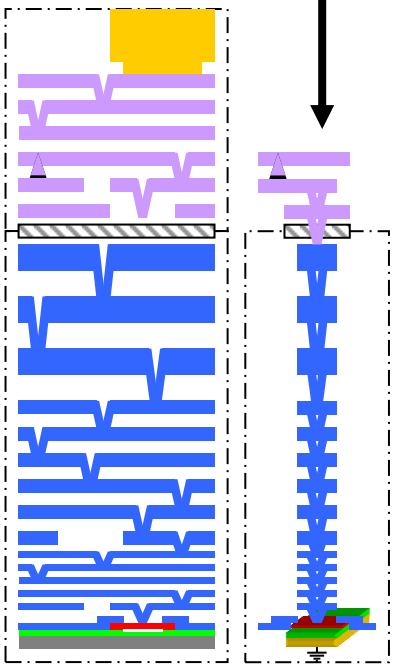


Standing on the Shoulders of Dwarves

- If you stand on the shoulders of dwarves, you may end up below the level of the original giants
- Need a “latency tolerant architecture”

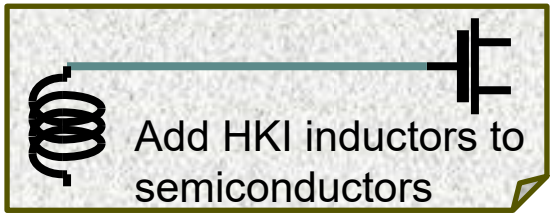


- Monolithic integration:
  - Superconductor
  - Semiconductor
- Deposit semi-conductor?
- Back-end-of-line supercon-ductor



Mine the Hybrid to Enhance CMOS or JJs

- Add variable capacitors to the JJ process
  - Variable capacitors are called varactors
  - Most CMOS processes have varactors
- Add HKI inductors to CMOS
- Example



Monolithic vs. Other Hybrid Fab Status

Monolithic hybrid

- Fabs: “no problem”
- Skeptics: “materials problems”
- MIT-LL made a monolithic hybrid
  - JJs and transistors worked, so no major materials problems
  - Turning on the transistors overheated the JJs and they stopped working
  - Emphatic it was a design issue
  - Verbal information only

Bumps and interposers

- MIT-LL Superconducting Multi-Chip Module (S-MCM)
- Excellent quality transmission lines

Design Principles for JJ CMOS Hybrids

Which layer for a functional block?

- If a block is too big, move it to the semiconductor base
- If a block dissipates too much heat, move it to the JJ layer
- Note: Requires a computer architect

Novel circuits spanning both layers

- Nobody has thought of them before because they could not be fabricated, so
  - Unexpected capability
  - More likely to be publishable, patentable, or a competitive differentiator

Part 2: Example of a Novel Circuit

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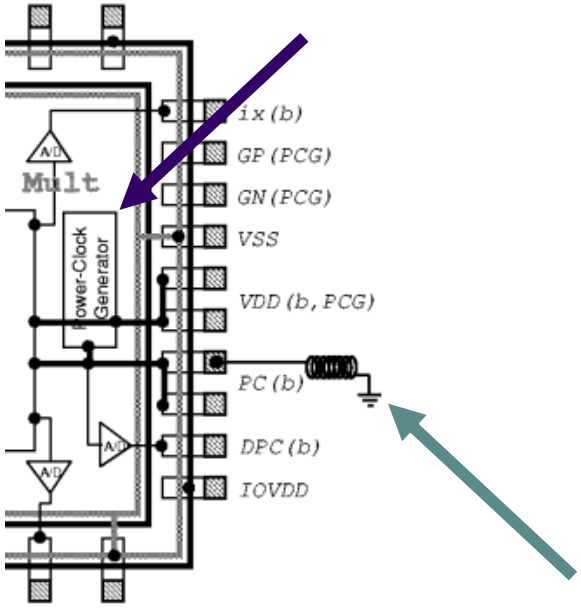
Reversible Semiconductor Logic, a Novel Circuit Class (I)

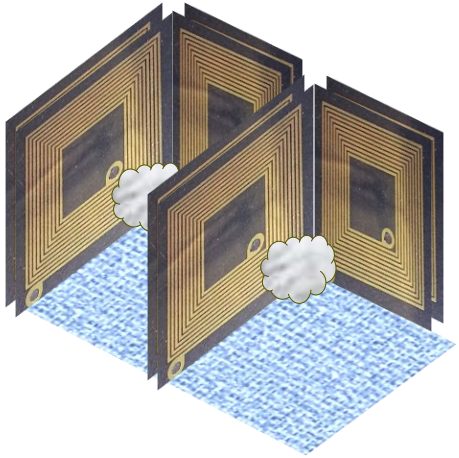
- CMOS circuit → reversible circuit
  - Switch logic gate circuits
  - Retain the functional block structure, busses, and long wires
- Power and clocking
  - In CMOS all energy goes in electrically and leaves as heat
  - In a reversible circuit (at 1 GHz), energy goes in during the 1st half of
  - each nanosecond and 90% - 99% comes out in the 2nd
  - Waveforms and energy recycling

Reversible Logic Story, with Scale up Chapter

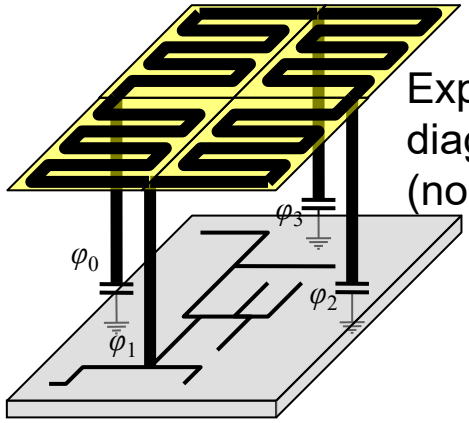
<u>300 K: Metal inductors</u>
Typical diagram below; External inductor



<u>77 K: High Tc inductors</u>
Geometric inductors require absence of conductors in surrounding space



<u>4 K: HKI induct-ors</u> Diagram exploded; actually monolithic
No need for empty space, so multiple layers possible



Exploded diagram; (no gap)

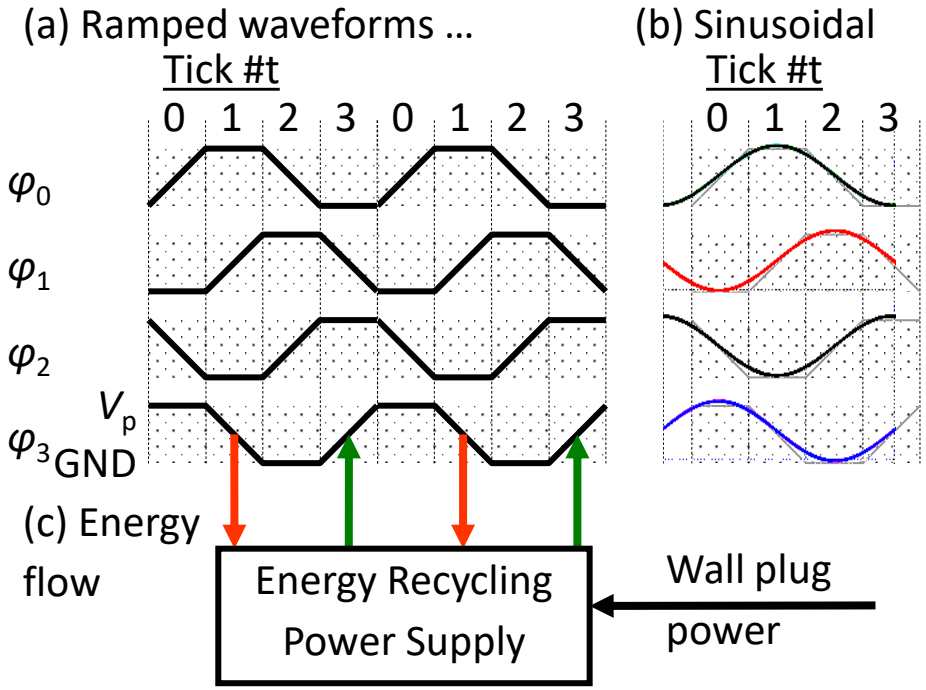
(left →) Power-clock generator
(right →) external inductor

(blue) array of rev. logic semiconductor chips
(gold) YBCO inductors

(yellow) HKI inductor layer
(gray) Semiconductor base

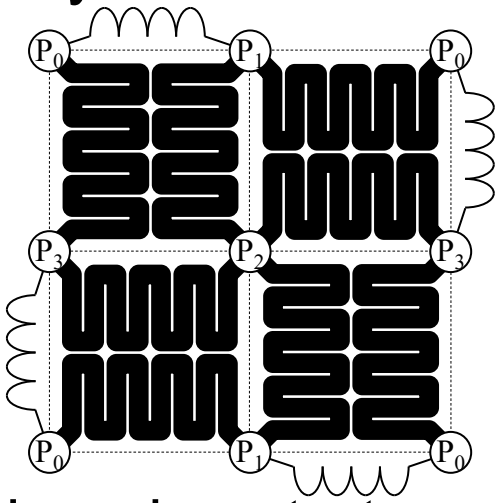
Reversible Semiconductor Logic, a Novel Circuit Class (II)

- CMOS circuit → reversible circuit
  - Switch logic gate circuits
  - Retain the functional block structure, busses, and long wires
- Power and clocking
  - In CMOS all energy goes in electrically and leaves as heat
  - In a reversible circuit (at 1 GHz), energy goes in during the 1st half of each nanosecond and 90% - 99% comes out in the 2nd
- Waveforms and energy recycling:



What is the Criteria for Getting Reversible Logic Unblocked?

- Diagram shows single HKI layer



- Engineering strategy:
  - Energy/unit area must be the same for inductance at I_{max} and capacitance at V_p.

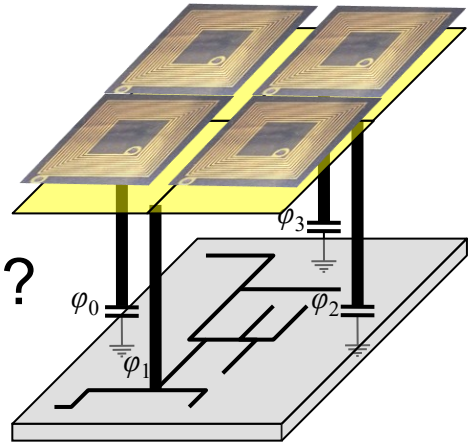
- HKI energy content
  - SeeQC: $L_{\square}$ = 8.5 pH/□, I_c = 2.5 mA/μm = 2500 A/m
  - For square dimension *s* x *s*:
  - Energy in an inductor: $\frac{1}{2}LI^2 = \frac{1}{2} L_{\square} (I_c s)^2 / s^2$ (*s*'s cancel) = .3 nJ/chip or 470 mW/chip at 1.6 GHz (1 cm^2 chip)
  - Horse Ridge (4x4 mm): 10-140 mW → 62–875 mW/cm^2
  - So, need 2 HKI layers
  - Ref. https://www.eetimes.com/intels-horse-ridge-ii-improves-the-control-for-quantum-computing/

YBCO/77 K Option

A Very Raw Direction for 77 K

- Diagram includes not-to-scale YBCO inductors ref. https://link.springer.com/content/pdf/10.1007/s00340-016-6430-z.pdf
- YBCO inductors have plenty of power density and Q
- YBCO needs empty space around it, but could the space be on just one side?
- May be useful for DARPA LTLT
- Hats off to Robin and STAR Cryo

77 K: High-Tc inductors Geometric inductors require absence of conductors in surrounding space – but how about on just one side?



(gold) YBCO inductors
(yellow) YBCO GND plane
(gray) semiconductor base

Conclusions on HKI for Reversible Logic

Claim: HKI “unblocks” reversible logic and it is now possible to convert practical cryo CMOS to reversible logic using JJ CMOS fab

- A hybrid chip could have regions containing reversible semiconductor logic, JJ logic, cryo CMOS logic, analog circuitry, etc.
- May increase energy efficiency over cryo CMOS by 10-100x
- Two layers of HKI possible. The method used for 3D flash may allow hundreds of layers, allowing more computational density
- I have ideas for 77 K operation, see me later
- I make no claim of an imminent room temperature solution