JCMOS: Josephson-CMOS hybrids

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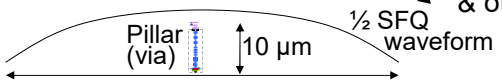
Note: Since selecting the title, I have discovered that a “monolithic hybrid” is often shortened to “monolithic” rather than “hybrid.” So, perhaps the title should have been “JCMOS: Josephson-CMOS monolithic integration.”

Outline: Add Focus and Detail to Integration Vision

- Josephson-DRAM integration + 6G Telecon GaAs-CMOS & other exotic transistors



Function	JCMOS	6G
THz Gain	JJ/SFQ	GaAs FET, etc.
Complex control	CMOS	CMOS

- Circuits with JJs and any of the devices in CMOS (varactor, Flash…)
- Novel circuits with varactors (S2C, S2SFQ, JJ FPGA)
  - Varactors are novel; concept applies to other devices as well
- Reduce dissipation of CMOS
  - Main trick: My circuits are useful with the clock stopped
- Applications examples FPGA vision and a scaled system vision

First bullet: The slide deck starts with Josephson-DRAM integration as pursued by various teams, including Van Duzer and Steve Whiteley, the previous speaker. The traditional approach is merged with the 6G telecom “roadmap.” 6G telecom is developing GaAs-CMOS hybrids to support THz radios. (GaAs is henceforth an expedient shortening of a list of about a half-dozen material combinations.)

The key technical concept is that a THz circuit requires wires to be shorter than about 10 μm, otherwise the wires turn into transmission lines and many circuits stop working. The diagram shows half-cycle of a THz sine wave (which looks pretty much like an SFQ pulse) with an at-scale depiction of a cross-technology via (that you will see in later slides).

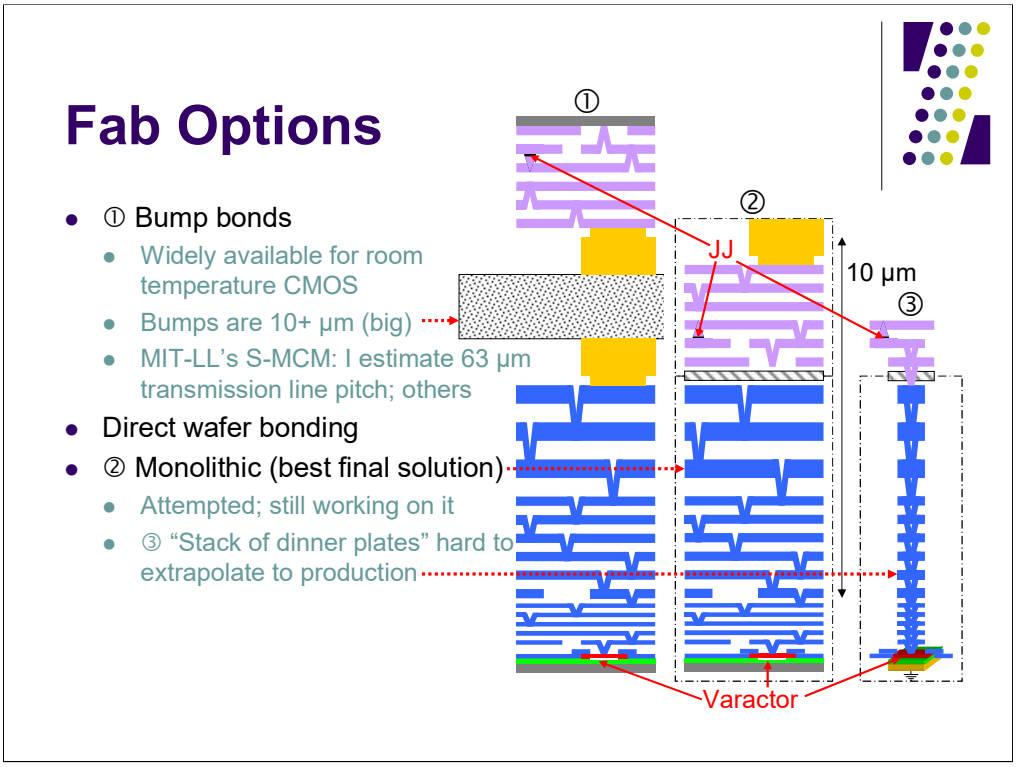
The merged vision would be a cryogenic THz-hybrid hybrid where JJs producing SFQ pulses are analogous to the exotic FETs. CMOS provides sophisticated control in both cases.

Second bullet. I have pointed out to colleagues that once Josephson-DRAM hybrids are readily available, designers will realize the can design circuits with JJs and any combination of devices in the CMOS process. This will enable more circuits and more applications. I find the point obvious, but colleagues seem to find it intriguing, so I emphasize this point.

Third bullet. I include several novel circuits in this talk. I base these circuits on a varactor.

Fourth major bullet. I am frequently asked about whether the “excessive” dissipation of CMOS will overheat the JJs and make hybrid stop working. Changing threshold voltage and reversible logic can help, but the main new point in this talk is that I am presenting new circuits that work with CMOS at 0 Hz clock rate for extended periods. CMOS leakage power is lower than is possible with the other approaches.

Fifth major bullet. I include applications example and a full system vision



① illustrates bump connections. The blue stack is Google's open (Sky130) CMOS stack and purple is a MIT-LL superconducting stack. ① shows separate CMOS and a superconducting stack fabricated separately. The superconducting stack flipped over and the two are connected with bump bonds. This could work, but the bump bond is pretty big. MIT-LL has a superconducting multi chip module (S-MCM), which can move SFQ pulses through superconducting wires (but the actual bumps are normal metal).

I think bump bonding could be used for near term demonstrations, but I do not think it is a long-term solution.

② illustrates monolithic integration. Basically, JJs are fabricated as Back and of Line (BEOL) on a CMOS chip. I know fabs that have attempted this, but are not publicizing the results. I think the monolithic approach will evolve into a long-term solution.

③ Using PowerPoint, I have extracted the basic structure of a JCMOS via, including materials and scale. It looks like a stack of dinner plates. I believe ③ is a useful diagram, but a lot of improvements are possible.

Semiconductor to Capacitance S2C Example of a Novel Signal

Novel analog signal

- To communicate *v* in CMOS
- Compute *C* = *f*(*v*) for varactor transfer function *f*
- Send *C* to the superconductor circuit

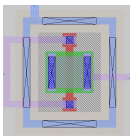
One option is to use signal directly

- Convert *C* to time
- Use in a semiconductor-controlled SFQ voltage controlled oscillator

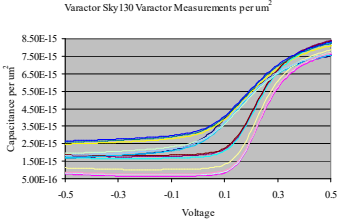
Another option would be to recover *v*

Backup: Varactors

- Example of a varactor layout



- Varactor transfer function *f*



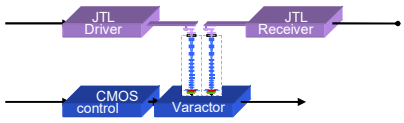
S2C is a novel circuit that transmits data from CMOS to superconducting devices using capacitance as a data variable. I believe this novel approach will be most useful where a JJ circuit can use the capacitance directly. The benefit will be to reduce the CMOS dissipation and the area used in the superconductor layer.

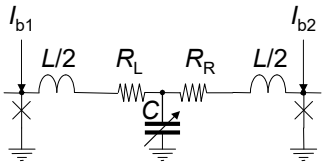
A voltage *v* present on the CMOS later is converted to capacitance by a varactor. A varactor layout is on the upper right of the slide and the transfer function on the lower right (the multiple transfer function curves are based on different parameter sets). The varactor's capacitance is between ground and a wire (pillar) that is available to the superconducting circuit.

A potential use case is for the superconductor circuit to translate the capacitance into time or frequency, leading to a voltage-controlled oscillator (VCO) controlled by *v* in the semiconductor layer.

S2C Block Diagram Analysis

- *C* affects the SFQ pulse
  - SFQ pulse goes down a JTL
  - Signal tapped and sent to *C*
  - If *C* is low, tap has little effect
  - If *C* is high, tap is a low pass filter
  - Hand waving analysis says the tap will delay or block the SFQ pulse (analysis inadequate, so go to next slide)





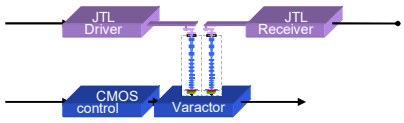
The S2C circuit is a JTL transmission line (in purple at the bottom) that has a tap. The tap connects to the varactor via pillars.

If the varactor has a small capacitance, the circuit is a JTL with a resistor, which is still a JTL.

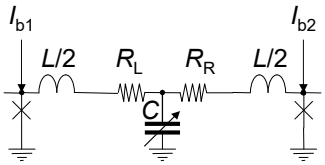
If the varactor has a large capacitance, the varactor become part of a low-pass filter. Hand-waving analysis suggests the low-pass filter will reduce the amplitude and delay the SFQ pulse – thus delaying recognition of the pulse by the right hand “JTL receiver” circuit.

S2C Circuit Analysis

- It's a resonant circuit
  - Left JJ produces a sharp pulse (delta function) that puts energy *E* in the left inductor. There no energy in *C*, so *E* does not depend on *C*
  - The RLC circuit resonates due to energy *E* at $f = 1/(2\pi\sqrt{LC})$. The top half of the sine wave will be like an SFQ pulse



- A higher varactor control voltage will create a higher varactor capacitance, making the period of the sine wave longer, making the JTL receiver trigger later and delaying the SFQ pulse



Circuit analysis:

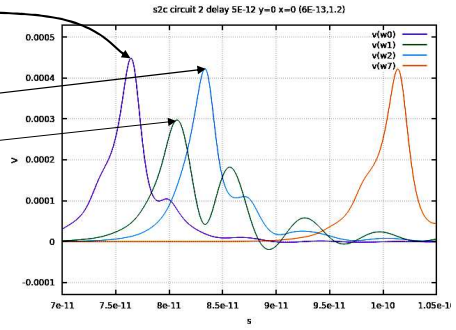
If the incoming JJ is treated as a delta function, it will deposit energy in only the left inductor. Since no energy is deposited in the capacitor at this point, the fact that it is a variable capacitor makes no difference.

Once the delta function passes, the left side of the schematic is a resonator that will (start) oscillating at $f = 1/(2\pi\sqrt{LC})$. Note that this would not be true if the wires connecting the resonator were transmission lines. Also note that the filter has a Tee structure. After a cycle or two, the second inductance will take effect and the frequency will decrease.

If the circuit equations were analyzed in more depth, the quantitative change in varactor triggering time would be computable.

S2C Simulation *C* = 0.6 pF

- Probe pulse
- Simulation at varactor *C* = 0.6 pF, 1.725 pF, and 2.85 pF
- Output
- Resonance
- Circuit rings down, should have *Q* = ~6



Advance slide to see capacitance sequence

This and the next two charts show:

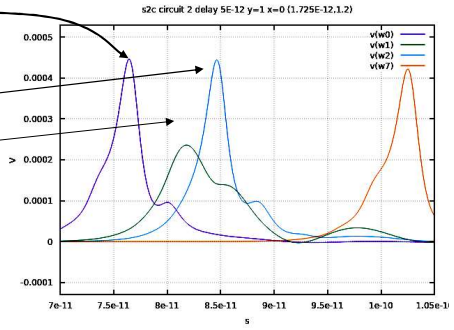
The purple input pulse (probe pulse) stays put. It is the reference.

The third green curve is the resonance. A view will see the wavelength increase from slide to slide – which is about all you can get from the slides.

The intermediate blue curve is the output. The delay increases as you move from slide to slide.

S2C Simulation *C* = 1.7 pF

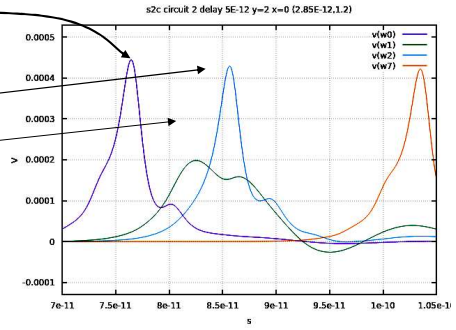
- Probe pulse
- Simulation at varactor *C* = 0.6 pF, 1.725 pF, and 2.85 pF
- Output
- Resonance
- Circuit rings down, should have *Q* = ~6



Advance slide to see capacitance sequence

S2C Simulation *C* = 2.85 pF

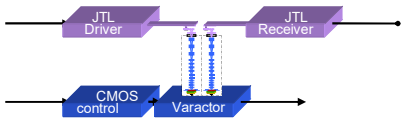
- Probe pulse
- Simulation at varactor *C* = 0.6 pF, 1.725 pF, and 2.85 pF
- Output
- Resonance
- Circuit rings down, should have *Q* = ~6

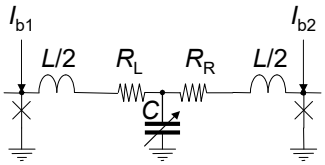


Advance slide to see capacitance sequence

S2C Energy Consumption

- Depends on how rapidly the control voltage changes
  - If the delay does not change, the CMOS can be static, so dissipation is CMOS leakage + a few SFQ pulses
  - If the delay changes rapidly, the CMOS control circuitry will be the dominant dissipation

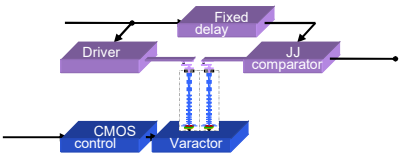


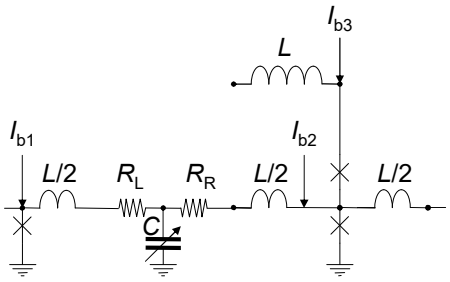


(No additional comments)

Semiconductor to SFQ (S2SFQ) Digital Link Example

- S2C circuit with digital input; pulse is either early or late
- Replaces receiving JTL stage with a JJ comparator
- Energy consumption: If input does not change, dissipation is
  - CMOS static leakage
  - SFQ pulses





S2SFQ is an extension of S2C just presented.

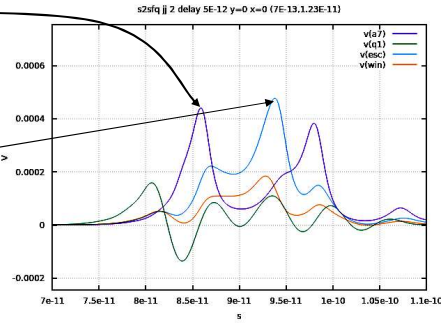
First, S2SFQ is a digital circuit, so only two values of *v* and capacitance are considered. The circuit produces (pretty much) the same resonance curves as the S2C circuit previously, but there are only two relevant curves (you can call them “early” and “late” SFQ pulses).

Second, the right JTL stage (called JTL receiver) has been replaced with a JJ comparator. The comparator inputs are the probe pulse with a fixed delay and the early/late pulses that have been influenced by the varactor.

S2SFQ Comparator 0.7 pF

- Probe pulse
- Simulation at varactor *C* = 0.7 pF, 1.42 pF, 2.1 pF, and 2.85 pF
- Comparator output (or not)

- Details:
  - Arrows stay put
  - Probe pulse experiences some back action
  - Output pulse definitely disappears, but is not totally stable when present



Advance slide to see capacitance sequence

This and the next three charts show:

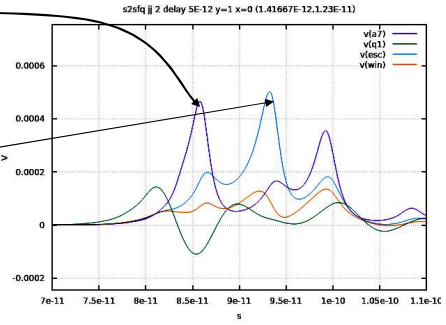
The original probe pulse in purple, which does not move.

The output of the JJ comparator in blue. The blue curve shows a pulse at about the same time in the first two charts, but no pulse in the second two charts. So, the circuit converts *v* as a digital signal to an SFQ signal output (pulse for 1 and no pulse for 0).

S2SFQ Comparator 1.42 pF

- Probe pulse
- Simulation at varactor *C* = 0.7 pF, 1.42 pF, 2.1 pF, and 2.85 pF
- Comparator output (or not)

- Details:
  - Arrows stay put
  - Probe pulse experiences some back action
  - Output pulse definitely disappears, but is not totally stable when present

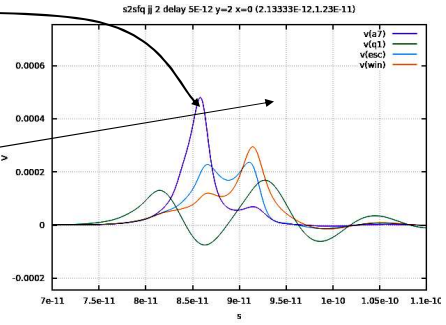


Advance slide to see capacitance sequence

S2SFQ Comparator 2.13 pF

- Probe pulse
- Simulation at varactor *C* = 0.7 pF, 1.42 pF, 2.1 pF, and 2.85 pF
- Comparator output (or not)

- Details:
  - Arrows stay put
  - Probe pulse experiences some back action
  - Output pulse definitely disappears, but is not totally stable when present

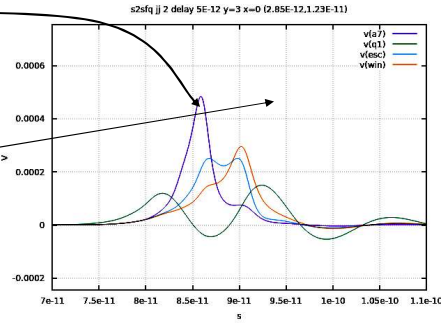


Advance slide to see capacitance sequence

S2SFQ Comparator 2.85 pF

- Probe pulse
- Simulation at varactor *C* = 0.7 pF, 1.42 pF, 2.1 pF, and 2.85 pF
- Comparator output (or not)

- Details:
  - Arrows stay put
  - Probe pulse experiences some back action
  - Output pulse definitely disappears, but is not totally stable when present



Advance slide to see capacitance sequence

Summary on Reducing CMOS dissipation

- Architectural
  - Where possible, shift activity to the SFQ circuitry
  - Turn off CMOS switching (0 Hz clock)
- MOSFET threshold voltage
  - For 4 K operation, doping levels can be changed to reduce threshold to about 40% of the room temperature value (reduces power by ~7x)
- Cryogenic reversible logic
  - Also a possibility, but details beyond talk's time limit
  - Reversible logic at room temperature needs an energy recycling power supply, which has never been perfected. This component not needed in cryogenic operation. The energy efficiency improvement could be up to ~100 x at 4 K.

This slide summarizes the CMOS dissipation issues:

The new point introduced in this slide deck is that the JJ + varactor circuits in this slide deck can process an arbitrarily large number of SFQ pulses even though the CMOS has a 0 Hz clock. CMOS static dissipation is far lower than dynamic dissipation, so this will reduce dissipation.

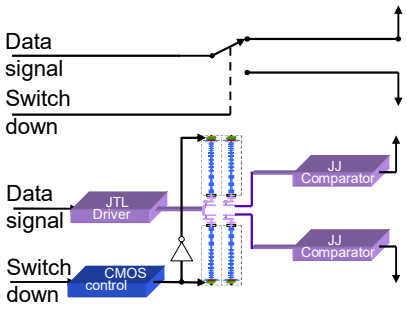
In fact, CMOS static dissipation is should be lower, or at least as low as, the dissipation of cryo CMOS with lower threshold voltages and reversible logic.

The reduced dissipation will not occur in all use cases. There are many use cases where the novel circuits in this slide deck will not offer an advantage. There will also be use cases where cryo CMOS with lower threshold voltages and reversible logic will not help either.

Application: SPDT Switch to Mitigate Obsolescence

SPDT switch shown below

- CMOS control selects “switch up” vs. “switch down”
- Data signal routed up or down depending on switch



Use Cases

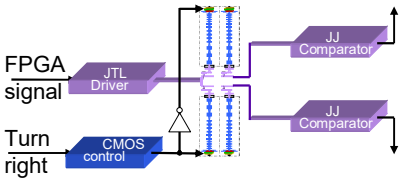
- Use in conjunction with a (personal computer) BIOS equivalent to mitigate obsolence
- Could be used during run time for “testing and calibration” vs. “normal execution” modes

A SPDT switch for SFQ pulses applies to many use cases. The lower block diagram shows two instances of S2SFQ, one mirrored vertically, and provided with the inverse control signal.

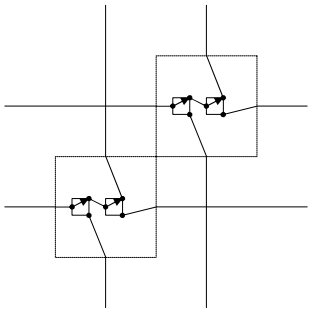
The upper diagram shows the equivalent SPDT switch (in this case, the SPDT switch works only for SFQ pulses flowing left-to-right).

JJ FPGA Use Case

- FPGAs have “programmable wiring network” that can connect gates in an array into any circuit
- During power up they set “programmable wiring” from a securely downloaded file



- Example wiring network element created from SPDT switches
- Rightward-flowing signals can “turn left” and “turn right”



An SPDT switch can be the key element in an FPGA.

This diagram shows the same SPDT switch as the previous slide.

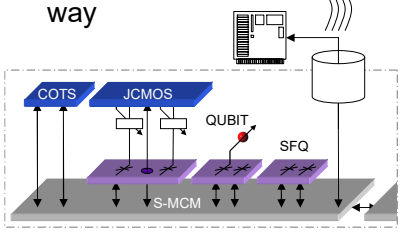
An FPGA includes a programmable wiring network, with two simple cross points are shown on the right. An FPGA wiring network can be illustrated by and array of the structures. Each repetition has horizontal and vertical wires where a left-to-right wire can be routed to a upwards or downwards wire based on the settings of SPDT switches.

(The diagram shown only illustrates horizontal to vertical connections. A programmable wiring network would need to include routing signals from each of the four Cartesian directions all the others.

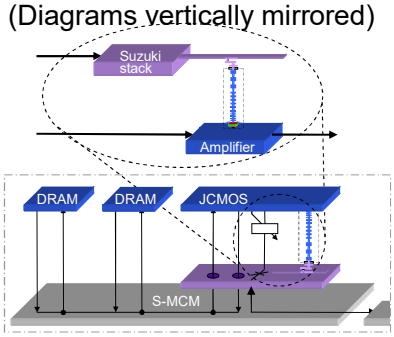
General System Vision and SFQ-DRAM Hybrid

General system vision

- JCMOS, all-JJ, all-CMOS, and qubit chips bonded to one or more connected S-MCMs
- Functions that can be performed by non-JCMOS are certainly cheaper to do that way



- Josephson-DRAM vision
- Can be seen as a smoother implementation of Whiteley's (van Duzer's) demonstration
- (Diagrams vertically mirrored)



This slide show two additional use cases for completeness.

The left shows the scale up vision for a general system. Technology like MIT-LL's S-MCM would provide high level connectivity of SFQ signals via superconducting transmission lines (CMOS voltage signals are implicitly included). However, this slide deck shows smaller scale wire-like connections (i.e. not transmission lines) as connections within JCMOS hybrids.

For cost optimization, all-semiconductor and all-SFQ chips could be mounted on the S-MCM as well. In fact, Qubit chips could be included.

The diagram also show a cryostat, cryocooler, and external electronics.

The right shows compatibility with past Josephson-DRAM hybrids, such as Van Duzer/Whiteley (previous speaker). This previous integration project included Suzuki stacks and semiconductor amplifiers. These circuits could be placed in the purple and blue blocks of S2SFQ circuit and should work equally well. However, this slide deck provides a path to improve on the past work. Specifically, the height of the Suzuki stack could be reduced due to lower loading of the pillars compared to bonding wires. The timing on the amplifier could be tightened up due to smaller time variance in JCMOS compared to bonding wires due to higher precision manufacturing.

Conclusions and Future Work

Conclusions

- Merged Josephson-DRAM agenda with 6G Telecon GaAs-CMOS hybrids to create JCMOS
  - JJs in equivalent role of exotic transistors
  - Clarifies support of THz circuits, not just transmission lines
- Demonstrated JJ-varactor circuits
  - These circuits can be helpful with CMOS running at a 0 Hz clock rate

Future Work

- More circuits. If you liked the talk, think about circuits with JJs and Flash or memristors
- Better interconnect. Devise better pillars, simulate with HFSS, and test them 
- Convince a fab to make monolithic stacks; including improved pillars

(No additional comments.)