

Rebooting Quantum Computing

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Rebooting Computing
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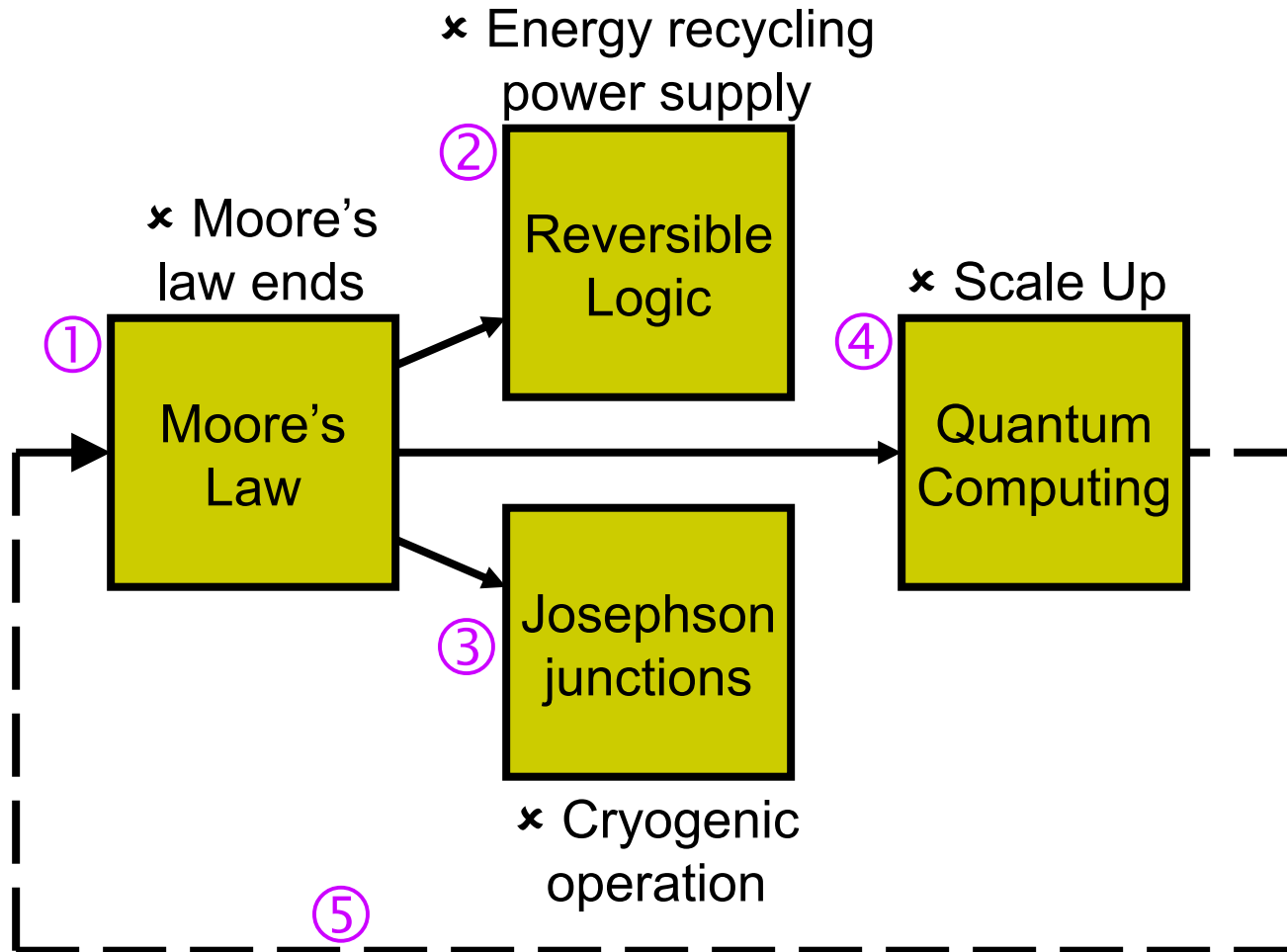
Technical Problem: Excessive Power Bill



- Scale up of superconducting quantum computers is encountering technological challenges
 - Google's milestone 6 is a million qubits in a structure that looks bigger than 10 meters of A380 fuselage (possible hidden slide)
 - IBM's roadmap mentions "millions of qubits"
 - But more is needed: a well-known quantum factoring paper calls for 20 million raw qubits
- Problem 1: No technology can run a million cables into a cryostat
- Problem 2: Excessive power bill for cryo-CMOS controllers at 4 K
 - IBM and Intel have cryo-CMOS controllers at 25 mW/qubit 4 K
 - Multiplying by a million and then 200× cryocooler overhead gives 5 MW
 - At \$1/watt-year,[†] the power bill will be \$5M/year for a million qubits and \$100M/year for 20 million qubits
- Rebooting Computing could hold conferences and publish results contributing to a solution

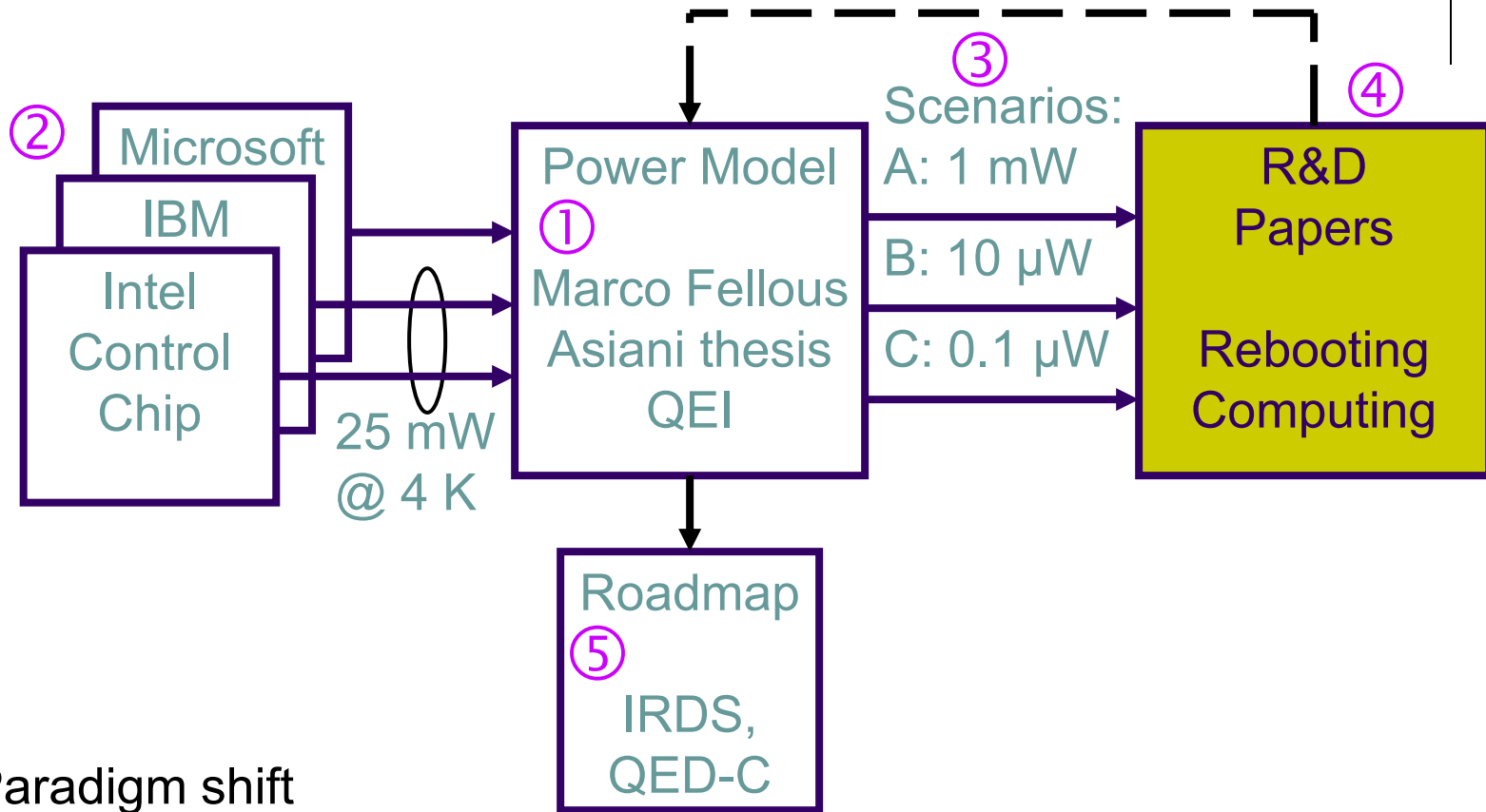
[†]12¢/kWh × 8766 hrs/year → \$1.05/W-year

Rebooting Computing Becomes an Infinite Loop





Details of the Second Reboot



Paradigm shift

- Previously, physics informed engineers of the temperatures
- In future, temperatures will be selected by an optimization algorithm

Hybrids and Technology Teamwork



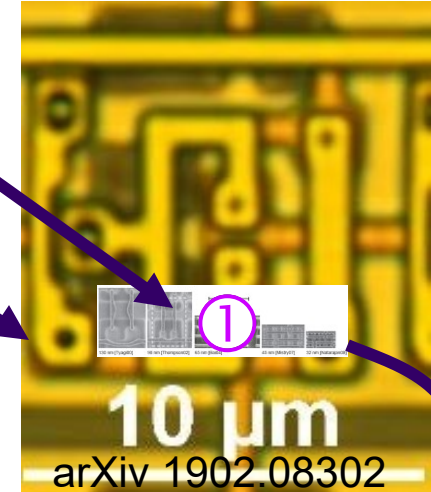
- Rebooting computing was organized like a horse race
 - Horses were named New Switch, Reversible, SFQ, ... (see hidden slide)
 - Horse with best performance parameters, get research funding by reduction in budget for the losing horses; teaming would not help
- Different approach in production (Smartphones)
 - Horses are CMOS, DRAM, Flash, RF, etc.
 - Smartphone manufacturer wants a team of horses that can expand the total money supply
- Quantum computers now have a goal, so Rebooting Computing could use the teaming approach

Example: Semiconductor-Superconductor Hybrid



- Horse 1: You can make a transistor chip
 - And people have done this
 - For detail, see ②; transistor are small
- Horse 2: You can then evaporatively deposit JJ/SFQ circuits
 - Would not look like this; layers reversed
- However, there is a size disparity
 - CMOS excels on density (size)
 - JJ/SFQ circuits are intrinsically fast and low power
- Can we use these horses in a team?

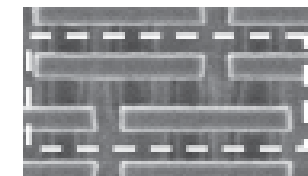
JJ SRAM cell



③

CMOS SRAM cell

②



32 nm [Natarajan08]

1 μm

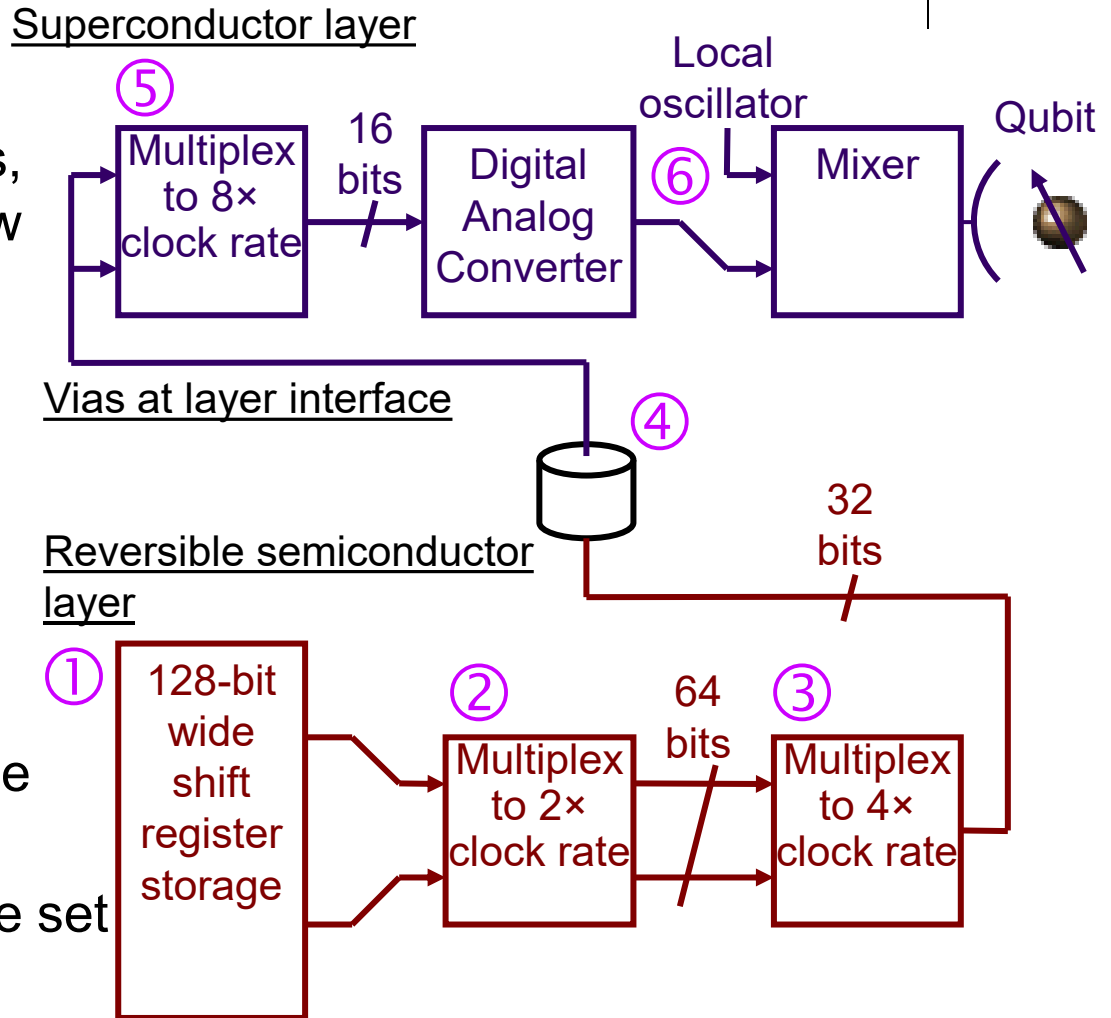
CMOS VLSI Design,
Weste

Semi- Superconductor Hybrid for Waveform Playback



Design concept

- Store data in transistors, which are small but slow
- Process data in JJs, which have low dissipation even at high speed
- Benefit: do not need single technology to be best at everything
- Cost: Need to design the interface
- But will need a complete set of functions





Quantum Roadmap

We now have a basis for an ITRS/IRDS-like roadmap

- Start with 25 mW/qubit and use framework to quantify how much each advance reduces the power of a quantum computer

Description	2022	2025	2030	2035	units
General factors					
Cryo-CMOS baseline power/qubit at 4 K	25 ①	25	25	25	mW
Cooling overhead to 4 K, large scale	200	200	200	200	W/W
Cryo-CMOS (not including this work)					
Process technology factor					
Example: 22FFL to GAA 3 nm			5 ②	5	×
Design optimization factor					
DAC, DSP improvements			10 ③	10	×
Rearchitect				5	×
Power per qubit @ 4 K	25,000	25,000	500	100	μW
Million qubit control system power	5,000	5,000	100	20	kW
Reversible logic (addon for this work)					
Circuit improvement over cryo-CMOS	1	25 ④	50	100	×
Power per qubit @ 4 K	25,000	1,000	10	1	μW
Million-qubit control system power	5,000	200	2	0.2 ⑤	kW

Summary



Technical material in this talk

- There is now a quantitative basis for roadmaps and benchmarks
 - Power prediction framework: Marco Fellous Asiani's thesis
 - Qubit controller chips: Intel, IBM, Microsoft; SeeQC
 - Quantum computers of growing size: Google, IBM, etc.
 - Source of new component technologies
 - Zettaflops, Hypres (us)
 - Rebooting Computing

Potential follow on activity

- IEEE has could support brainstorm type activity, which could be ICRC
- The prediction framework could become the basis of a roadmap like ITRS/IRDS
- Benchmarks could be created for subfunctions
 - Chip area and dissipation for the hybrid waveform playback using a reference waveform

Leave Behinds and Additional Information



The submitted paper and this PowerPoint (with hidden slides and references) are posted at

<https://www.zettaflops.org/ICRC-22>

It is a WordPress site, so you can go to zettaflops.org and use the site's navigation

Zettaflops, LLC and Hypres have applicable technology