Rebooting Quantum Computing

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Technical Problem: Excessive Power Bill

- Scale up of superconducting quantum computers is encountering technological challenges
  - Google's milestone 6 is a million qubits in a structure that looks bigger than 10 meters of A380 fuselage (possible hidden slide)
  - IBM's roadmap mentions "millions of qubits"
  - But more is needed: a well-known quantum factoring paper calls for 20 million raw qubits
- Problem 1: No technology can run a million cables into a cryostat
- Problem 2: Excessive power bill for cryo-CMOS controllers at 4 K
  - IBM and Intel have cryo-CMOS controllers at 25 mW/qubit 4 K
  - Multiplying by a million and then 200× cryocooler overhead gives 5 MW
  - At $1/watt-year,† the power bill will be $5M/year for a million qubits and $100M/year for 20 million qubits
- Rebooting Computing could hold conferences and publish results contributing to a solution

†12¢/kWH × 8766 hrs/year → $1.05/W-year

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References:

[1] Neven, Harmut, "Quantum AI Update," Google Symposium 2022, offset 15:00. https://eventsonair.withgoogle.com/events/qss-2022 (note: this link requires registration).

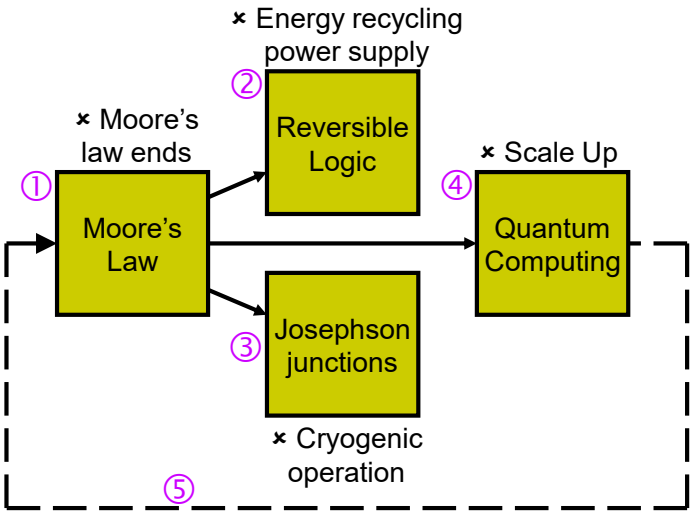
[2] Expanding the IBM Quantum roadmap to anticipate the future of quantum-centric supercomputing, https://research.ibm.com/blog/ibm-quantum-roadmap-2025.

[3] Pellerano, Stefano, et al. "Cryogenic CMOS for Qubit Control and Readout." 2022 *IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, 2022. DOI: https://doi.org/10.1109/CICC53496.2022.9772841 https://pure.tudelft.nl/ws/portalfiles/portal/122719163/Cryogenic_CMOS_for_Qubit_Control_and_ReadoutTaverne.pdf.

[4] Frank, David J., et al. "A Cryo-CMOS Low-Power Semi-Autonomous Qubit State Controller in 14nm FinFET Technology." *2022 IEEE International Solid-State Circuits Conference (ISSCC)*. Vol. 65. IEEE, 2022. DOI: https://doi.org/10.1109/ISSCC42614.2022.9731538.

[5] Frontier to Meet 20MW Exascale Power Target Set by DARPA in 2008 https://www.hpcwire.com/2021/07/14/frontier-to-meet-20mw-exascale-power-target-set-by-darpa-in-2008/.

Rebooting Computing Becomes an Infinite Loop



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* ① Rebooting computing redefined computing-related R&D priorities in response to the end of Moore's law.

* The new priorities directed attention toward ② reversible logic, ③ Josephson junction (JJ) electronics, ④ quantum computing, and other approaches.

* Reversible logic and JJs did not thrive for the reasons shown by the × symbols, but quantum computing has attracted substantial investment and is now undergoing scale up [1-2] in preparation for commercialization.

* Yet new data this year [3-4] shows that scale up of quantum computers will be dependent on reducing the dissipation of classical electronics, which is Moore's law. This would cause Rebooting Computing to "loop" ⑤ -- and IEEE might be able to "Reboot Computing" for decades into the future.

* The second reboot would be different. The first reboot targeted consumer electronics and included an unstated assumption everything would operate at room temperature, but the second pass would include cryogenic operation.

References:

[1] Neven, Harmut, "Quantum AI Update," Google Symposium 2022, offset 15:00. https://eventsonair.withgoogle.com/events/qss-2022 (note: this link requires registration).

[2] Expanding the IBM Quantum roadmap to anticipate the future of quantum-centric supercomputing, https://research.ibm.com/blog/ibm-quantum-roadmap-2025.

[3] Pellerano, Stefano, et al. "Cryogenic CMOS for Qubit Control and Readout." 2022 *IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, 2022. DOI: https://doi.org/10.1109/CICC53496.2022.9772841 https://pure.tudelft.nl/ws/portalfiles/portal/122719163/Cryogenic_CMOS_for_Qubit_Control_and_ReadoutTaverne.pdf.

[4] Frank, David J., et al. "A Cryo-CMOS Low-Power Semi-Autonomous Qubit State Controller in 14nm FinFET Technology." *2022 IEEE International Solid-State Circuits Conference (ISSCC)*. Vol. 65. IEEE, 2022. DOI: https://doi.org/10.1109/ISSCC42614.2022.9731538.

Backup 0:
RCS 4 Summary Report

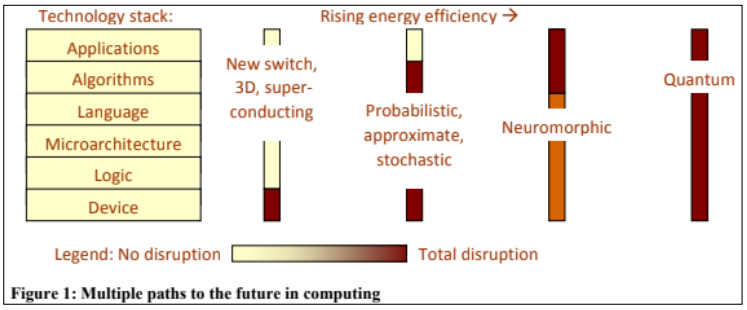


Figure 1: Multiple paths to the future in computing

Source:

RCS 4
4th Rebooting Computing Summit
"Roadmapping the Future of Computing"
Summary Report

3.1

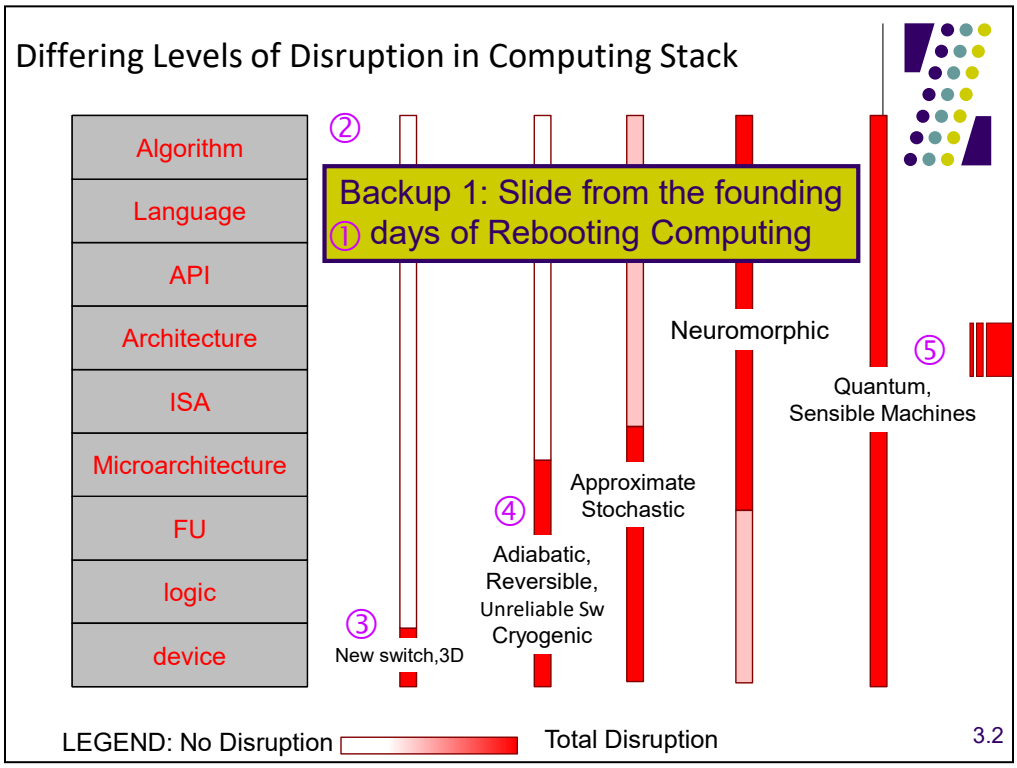
Historical interest only.

The report is not online at present.

Original file: RCS4 ver M 8.pdf attached to an email Sun, Jan 10, 2016, 9:39 AM from Erik DeBenedictis with subject "RCS 4 report -- ready for wider review," and starting with:

Hello Committee:

I'm attaching a draft RCS 4 report that that has made it through me, Dave, and Alan.

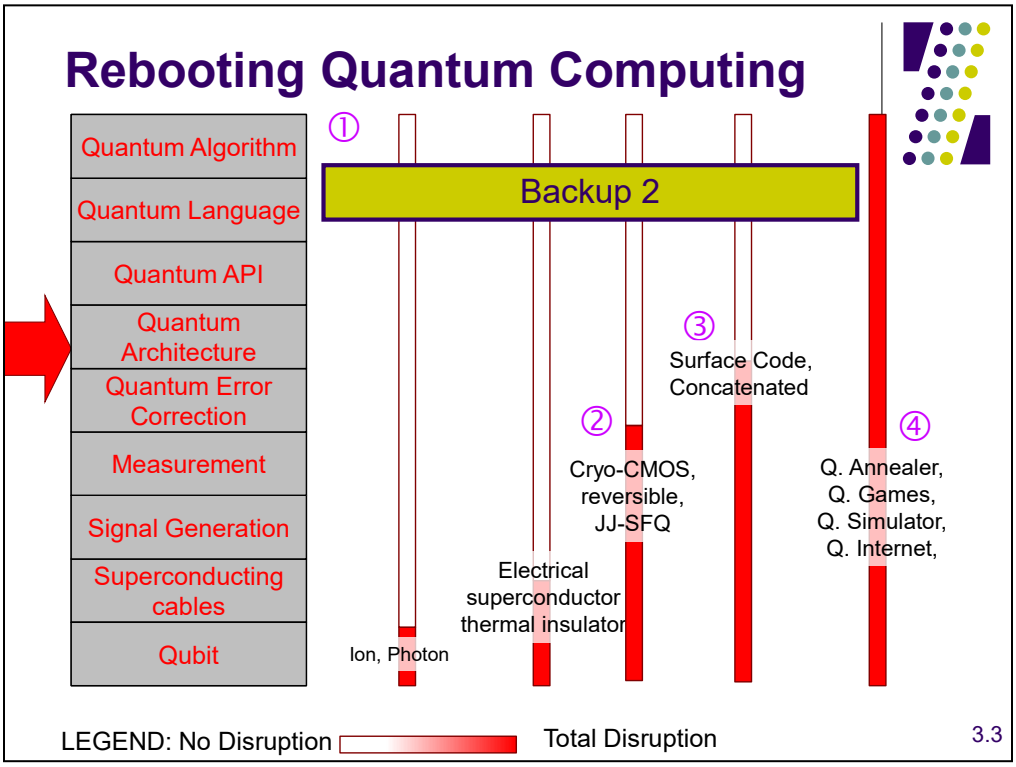


* ① This is a modified version of Erik DeBenedictis' diagram.

* "Computing," defined by the stack ②, needed a "reboot" so the Rebooting Computing Initiative was going to consider R&D in the "thermometers" to the right.

* The path of minimal disruption would be a "new switch" ③ that would allow Moore's law to continue its exponential path of improvement with little disruption. In retrospect, Moore's law slowed but continues in a weakened form.

* Rebooting Computing Initiative also considered reversible logic, Josephson junction (JJ) electronics ④, but they did not thrive.
* However, quantum computing, and "Sensible Machine" (which is Artificial Intelligence and neural nets) ⑤ have become forward-looking research priorities.

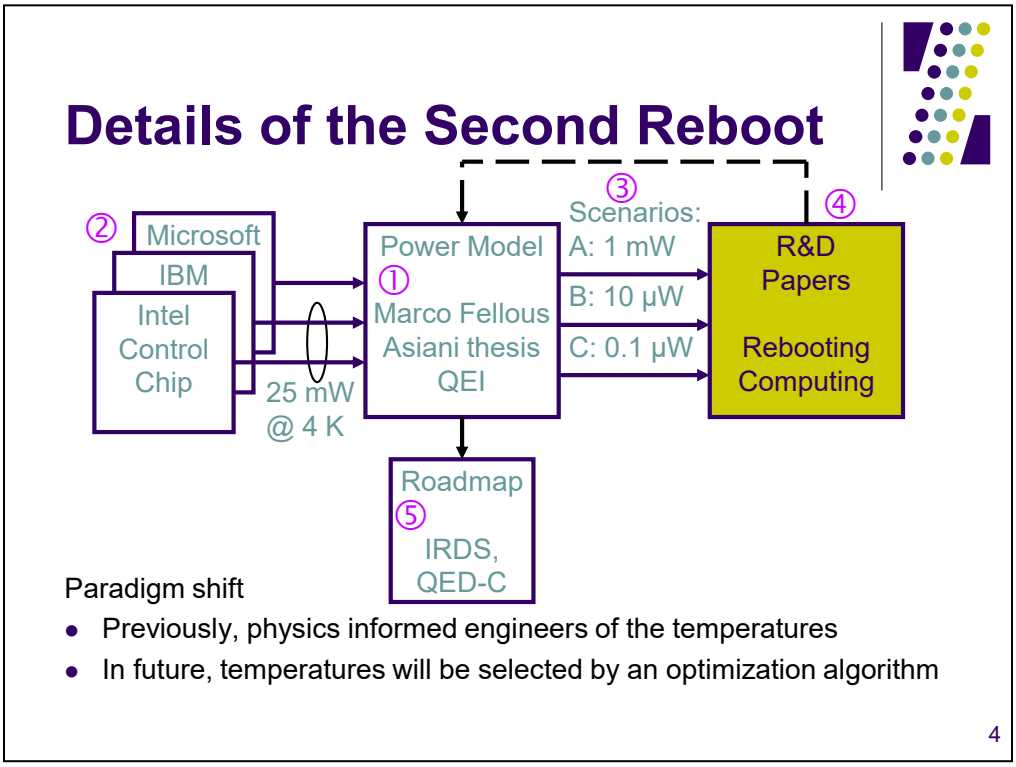


* For quantum computers to scale up will require a substantial improvement in the energy efficiency of classical electronics. At a high level, this is the same problem that Rebooting Computing solved, but for a different technology stack ① and different potential solutions ②③④.

* Some of the potential solutions are the same as the original reboot, such as “Adiabatic, Reversible, Cryogenic” (now “Cryo-CMOS, reversible and JJ-SFQ” ②)

* However, other aspects of quantum computing require new categories of technology, such as quantum error correction codes ③.

* Just as with the first reboot, continuation of the status quo would enable quick exit if qubits could be improved could lead to a disruptive third reboot if the non gate-model quantum computer were to give way to another type (quantum annealer, etc. ④).



① The new central component is a quantum power model [1], which is a set of equations that take (a) qubit parameters, (b) classical control parameters, (c) parameters for passives, such as superconducting cables, and (d) algorithm (or application) parameters and generate from these a model of a specific quantum computer. The equations also optimize the design, such as by identifying the best temperature of the qubits, control electronics, etc. The model will report such factors as number of qubits and power/energy to execute the algorithm.

② The equations must be calibrated to the current state of the art, which is possible with the recent chips from Intel [2], IBM [3], and Microsoft [4]. There is a less mature SFQ approach as well [5].

③ The power model deals with the future by scenarios A, B, and C, which are defined by power levels for control electronics similar to the published chips. (It should be noted that scenarios A, B, and C are defined only for signal generation power, whereas a future iteration should have other parameters as well.)

④ The opportunity for Rebooting Computing is to find improvements over the cryo-CMOS that reach the power levels of scenarios A, B, and C. Benchmarks on the improvements could then be plugged into the power model.

⑤ The approach could also lead to a quantitative roadmap, essentially the quantum equivalent of the ITRS/IRDS “More Moore” roadmap. (More on this in a later slide.)

References:

[1] Fellous-Asiani, Marco, et al. "Optimizing resource efficiencies for scalable full-stack quantum computers." *arXiv preprint arXiv*:2209.05469 (2022). https://arxiv.org/abs/2209.05469.

[2] Pellerano, Stefano, et al. "Cryogenic CMOS for Qubit Control and Readout." 2022 *IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, 2022. DOI: https://doi.org/10.1109/CICC53496.2022.9772841 https://pure.tudelft.nl/ws/portalfiles/portal/122719163/Cryogenic_CMOS_for_Qubit_Control_and_ReadoutTaverne.pdf.

[3] Frank, David J., et al. "A Cryo-CMOS Low-Power Semi-Autonomous Qubit State Controller in 14nm FinFET Technology." *2022 IEEE International Solid-State Circuits Conference (ISSCC)*. Vol. 65. IEEE, 2022. DOI: https://doi.org/10.1109/ISSCC42614.2022.9731538.

[4] Pauka, S. J., et al. "A cryogenic CMOS chip for generating control signals for multiple qubits." *Nature Electronics* 4.1 (2021): 64-70. DOI: https://doi.org/10.1038/s41928-020-00528-y.

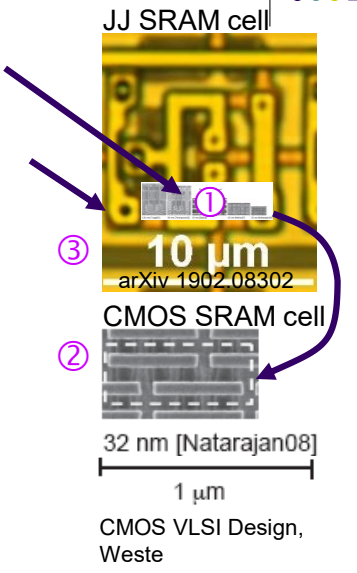
[5] Jokar, Mohammad Reza, et al. "DigiQ: A Scalable Digital Controller for Quantum Computers Using SFQ Logic." *2022 IEEE International Symposium on High-Performance Computer Architecture (HPCA)*. IEEE, 2022. DOI: https://doi.org/10.1109/HPCA53966.2022.00037 https://arxiv.org/pdf/2202.01407.

Hybrids and Technology Teamwork

- Rebooting computing was organized like a horse race
  - Horses were named New Switch, Reversible, SFQ, … (see hidden slide)
  - Horse with best performance parameters, get research funding by reduction in budget for the losing horses; teaming would not help
- Different approach in production (Smartphones)
  - Horses are CMOS, DRAM, Flash, RF, etc.
  - Smartphone manufacturer wants a team of horses that can expand the total money supply
- Quantum computers now have a goal, so Rebooting Computing could use the teaming approach

Example: Semiconductor-Superconductor Hybrid

- Horse 1: You can make a transistor chip
  - And people have done this
  - For detail, see ②; transistor are small
- Horse 2: You can then evaporatively deposit JJ/SFQ circuits
  - Would not look like this; layers reversed
- However, there is a size disparity
  - CMOS excels on density (size)
  - JJ/SFQ circuits are intrinsically fast and low power
- Can we use these horses in a team?



CMOS VLSI Design, Weste

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References:

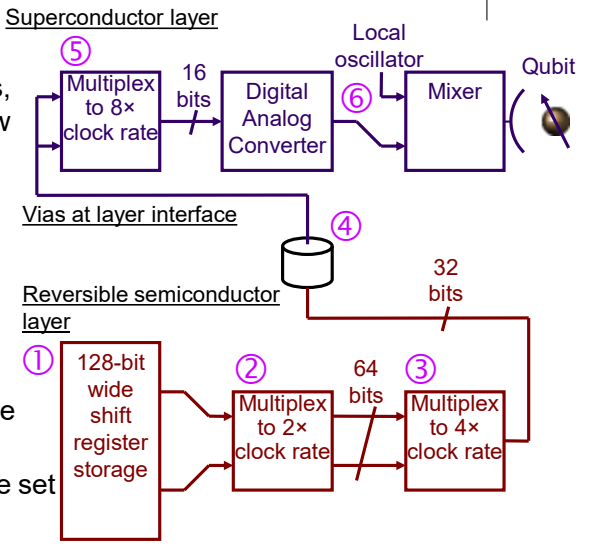
[1] Natarajan, S., et al. "A 32nm logic technology featuring 2 nd-generation high-k+ metal-gate transistors, enhanced channel strain and 0.171 μm 2 SRAM cell size in a 291Mb array." *2008 IEEE International Electron Devices Meeting*. IEEE, 2008.

[2] Semenov, Vasili K., Yuri A. Polyakov, and Sergey K. Tolpygo. "Very large scale integration of Josephson-junction-based superconductor random access memories." *IEEE Transactions on Applied Superconductivity* 29.5 (2019): 1-9.

Semi- Superconductor Hybrid for Waveform Playback

Design concept

- Store data in transistors, which are small but slow
- Process data in JJs, which have low dissipation even at high speed
- Benefit: do not need single technology to be best at everything
- Cost: Need to design the interface
- But will need a complete set functions



Signal generation is currently the pacing subcomponent for superconducting qubit quantum computers. The diagram is a potential hybrid implementation, which will be described in terminology similar to a memory subsystem.

* ① Data is stored in transistors whose principal feature is that they are small and hold a lot of data per unit of chip area. However, they must be run slowly to be energy efficient, but the low speed is offset by a wide width, 128 bits in this case.
* ② ③ ⑤ The overall system architecture then reduces the data width by interleaving and increases its speed, which can proceed through multiple stages [1].
* ④ At some point the information must be transferred to the superconducting JJ devices. Since transistors and JJs can be fabricated on the same chip, such as on different layers, the physical transfer mechanism is a standard via. There are circuits for changing signal voltage levels (which need further refinement).
* ⑥ Ultimately, the narrow, fast data stream can be turned into an analog waveform by a Digital-Analog-Converter (DAC) [2] or some other method [3].
* The novel feature is that the width and speed of the stream when it crosses the interface from transistors to JJs will affect the effectiveness of the resulting system. If the signal is too fast, the semiconductors will dissipate too much power, but if the signal is too wide, the number of JJs required will consume too much chip area.

References:

[1] DeBenedictis, Erik P. "Adiabatic circuits for quantum computer control." *2020 International Conference on Rebooting Computing (ICRC)*. IEEE, 2020. https://doi.org/10.1109/ICRC2020.2020.00004 https://debenedictis.org/erik/CATC/Log_Shift_Reg_v1.02.pdf.

[2] Sirois, Adam J., et al. "Josephson microwave sources applied to quantum information systems." IEEE Transactions on Quantum Engineering 1 (2020): 1-7. DOI: https://doi.org/10.1109/TQE.2020.3045682.

[3] Jokar, Mohammad Reza, et al. "DigiQ: A Scalable Digital Controller for Quantum Computers Using SFQ Logic." *2022 IEEE International Symposium on High-Performance Computer Architecture (HPCA)*. IEEE, 2022. DOI: https://doi.org/10.1109/HPCA53966.2022.00037 https://arxiv.org/pdf/2202.01407.

Quantum Roadmap

We now have a basis for an ITRS/IRDS-like roadmap

- Start with 25 mW/qubit and use framework to quantify how much each advance reduces the power of a quantum computer

Description	2022	2025	2030	2035	units
General factors					
Cryo-CMOS baseline power/qubit at 4 K	25 ①	25	25	25	mW
Cooling overhead to 4 K, large scale	200 ①	200	200	200	W/W
Cryo-CMOS (not including this work)					
Process technology factor					
Example: 22FFL to GAA 3 nm			5 ②	5	×
Design optimization factor					
DAC, DSP improvements			10 ③	10	×
Rearchitect				5	×
Power per qubit @ 4 K	25,000	25,000	500	100	µW
Million qubit control system power	5,000	5,000	100	20	kW
Reversible logic (addon for this work)					
Circuit improvement over cryo-CMOS	1	25 ④	50	100	×
Power per qubit @ 4 K	25,000	1,000	10	1	µW
Million-qubit control system power	5,000	200	2	0.2 ⑤	kW

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The ideas presented above could be used to create a quantum roadmap:

In a format similar to ITRS/IRDS, time moves horizontally and each column is a 1-D spreadsheet that computes a figure of merit for a point in time.

① Represents unchanging values or values decided humans based on intuition. In this case, the 25 mW in the published papers [1] [2] will be used as a baseline.

② Moore's law may have slowed, but it has not stopped. So, modest improvements in semiconductor parameters are included and will have a multiplicative effect (actually division) on the overall figure of merit. These advances would not be part of quantum computing R&D activities, but quantum computers would benefit.

③ An examination of [1] and [2] indicates that their design includes test structures (e.g. an instruction processor) that were useful in at the time but which could be removed in a production implementation. This is listed as 10×. A later set of improvements listed as 5× is on the roadmap too.

④ Reversible logic could be an advance as well, which the authors estimate has the potential for a 100× improvement, but this improvement may not appear all at once, so the row shows a growing sequence.

⑤ The ultimate roll up is the product of the first two lines ① divided by the values in the other lines ② ③ ④ (and multiplied by a million).

This point of the roadmap is that it combines improvement from many sources over time to yield a power reduction from 5 mW to 200 W, the former being a major corporate investment and the latter being reasonable for a single employee.

References:

[1] Pellerano, Stefano, et al. "Cryogenic CMOS for Qubit Control and Readout." 2022 *IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, 2022. DOI: https://doi.org/10.1109/CICC53496.2022.9772841 https://pure.tudelft.nl/ws/portalfiles/portal/122719163/Cryogenic_CMOS_for_Qubit_Control_and_ReadoutTaverne.pdf.

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Summary

Technical material in this talk

- There is now a quantitative basis for roadmaps and benchmarks
  - Power prediction framework: Marco Fellous Asiani's thesis
  - Qubit controller chips: Intel, IBM, Microsoft; SeeQC
  - Quantum computers of growing size: Google, IBM, etc.
  - Source of new component technologies
    - Zettaflops, Hypres (us)
    - Rebooting Computing

Potential follow on activity

- IEEE has could support brainstorm type activity, which could be ICRC
- The prediction framework could become the basis of a roadmap like ITRS/IRDS
- Benchmarks could be created for subfunctions
  - Chip area and dissipation for the hybrid waveform playback using a reference waveform

Leave Behinds and Additional Information

The submitted paper and this PowerPoint (with hidden slides and references) are posted at

https://www.zettaflops.org/ICRC-22

It is a WordPress site, so you can go to zettaflops.org and use the site's navigation

Zettaflops, LLC and Hypres have applicable technology

References from Paper

1. Neven, Harmut, "Quantum AI Update," Google Symposium 2022, offset 15:00. https://eventsonair.withgoogle.com/events/qss-2022 (note: this link requires registration).
2. Expanding the IBM Quantum roadmap to anticipate the future of quantum-centric supercomputing, https://research.ibm.com/blog/ibm-quantum-roadmap-2025.
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5. Fellous-Asiani, Marco. *The resource cost of large scale quantum computing*. Diss. Université Grenoble Alpes 2022. https://arxiv.org/pdf/2112.04022.pdf.
6. Fellous-Asiani, Marco, et al. "Optimizing resource efficiencies for scalable full-stack quantum computers." *arXiv preprint arXiv*:2209.05469 (2022). https://arxiv.org/abs/2209.05469.
7. Frontier to Meet 20MW Exascale Power Target Set by DARPA in 2008 https://www.hpcwire.com/2021/07/14/frontier-to-meet-20mw-exascale-power-target-set-by-darpa-in-2008/.
8. Feynman, Richard P. "Simulating physics with computers." *International Journal of theoretical physics* 21.6/7 (1982).
9. Fredkin, Edward, and Tommaso Toffoli. "Conservative logic." *International Journal of theoretical physics* 21.3-4 (1982): 219-253.
10. Younis, Saed G. *Asymptotically Zero Energy Computing Using Split-Level Charge Recovery Logic*. Diss. Massachusetts Institute of Technology, 1994. https://dspace.mit.edu/handle/1721.1/7058.
11. Lim, Joonho, Dong-Gyu Kim, and Soo-Ik Chae. "nMOS reversible energy recovery logic for ultra-low-energy applications." *IEEE Journal of Solid-State Circuits* 35.6 (2000): 865-875. DOI: https://doi.org/10.1109/4.845190 https://s-space.snu.ac.kr/bitstream/10371/16274/1/nMOS%20reversible%20energy%20recovery%20logic%20for%20ultra-low-energy%20applications.pdf.
12. Pauka, S. J., et al. "A cryogenic CMOS chip for generating control signals for multiple qubits." *Nature Electronics* 4.1 (2021): 64-70. DOI: https://doi.org/10.1038/s41928-020-00528-y.
13. DeBenedictis, Erik P. "Adiabatic circuits for quantum computer control." *2020 International Conference on Rebooting Computing (ICRC)*. IEEE, 2020. https://doi.org/10.1109/ICRC2020.2020.00004 https://debenedictis.org/erik/CATC/Log_Shift_Reg_v1.02.pdf.
14. DeBenedictis, Erik P. "*Classical Reversible Logic Circuits for Quantum Computer Control*," Zettaflops, LLC Technical Report ZF010. https://debenedictis.org/erik/CATC/MgtECompZF010v3.pdf.
15. Hornibrook, J. M., et al. "Cryogenic control architecture for large-scale quantum computing." *Physical Review Applied* 3.2 (2015): 024010 DOI: https://doi.org/10.1103/PhysRevApplied.3.024010 https://arxiv.org/pdf/1409.2202.
16. DeBenedictis, Erik P. Managing Energy in Computation with Reversible Circuits. Patent Application No. WO2022197556. September, 2022. https://patentscope.wipo.int/search/en/detail.jsf?docId=WO2022197556.
17. Sirois, Adam J., et al. "Josephson microwave sources applied to quantum information systems." IEEE Transactions on Quantum Engineering 1 (2020): 1-7. DOI: https://doi.org/10.1109/TQE.2020.3045682.
18. Jokar, Mohammad Reza, et al. "DigiQ: A Scalable Digital Controller for Quantum Computers Using SFQ Logic." *2022 IEEE International Symposium on High-Performance Computer Architecture (HPCA)*. IEEE, 2022. DOI: https://doi.org/10.1109/HPCA53966.2022.00037 https://arxiv.org/pdf/2202.01407.