Figure of Merit for Reversible Logic Systems

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ABSTRACT

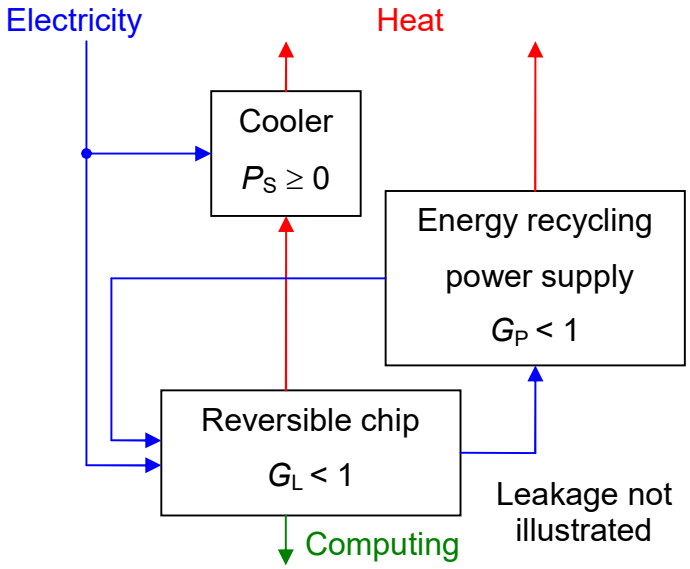
This document proposes a figure of merit R_{FOM} for transistor-based reversible logic. The belief is that reversible logic is ready for investment as a near-term opportunity, although there are also longer-term opportunities. As an example of the use of the figure of merit, investors expect a 10× improvement over the state of the art (CMOS) before funding product development, with this document providing a basis for such determinations.

This document proposes R_{FOM}, which is the overall wall-plug energy efficiency improvement factor for a reversible transistor circuit compared to CMOS. This would be a number > 1, e. g. R_{FOM} of 10 would indicate 1/10th the energy in comparison to CMOS for an equivalent function.

The original reversible logic concept depended on three factors, the $2RC/\tau$ energy factor of the logic, the efficiency of the energy-recycling power supply, and a dissipation floor that depends on static leakage. Recently, a cryo-adiabatic power train has been proposed that also depends on a cooling overhead.

INTRODUCTION AND REFERENCE MODEL

The reference model below shows reversible logic from the perspective of energy flow. The system is powered by electricity arriving from above (blue), which is all ultimately turned into heat (red), with the desirable side-effect of producing as much computing (green) as possible.



Reversible logic circuits eject a portion G_L of their input energy in a form that may be suitable for recycling. In the original formulation of reversible logic from the 1990s, recyclable energy was sent to an energy recycling power supply, which would send a portion G_P of the recyclable energy back to the chip. As will be explained below, the system-level energy efficiency rises toward a singularity as the product $G_L G_P$ approaches 1.

The reversible chip can run in a cryocooler, removing heat with an energy overhead factor, called specific power, P_S. Specific power is in units of Watts per Watt and is the amount of power that must be added per unit of power removed from the cryostat.

This document applies to both cryogenic and room temperature operation. If the reversible chip is in a cryostat, the energy overhead factor P_S should correspond to the cryocooler in use, otherwise use $P_S = 0$. Likewise, use $G_P = 0$ if there is no energy recycling. The figure of merit will accurately represent a system with both a cryocooler and an energy recycling power supply.

The objective of this document is to provide a figure of merit for a reversible logic system that includes the factors P_S, G_L, G_P, and the leakage parameters I_{off}/I_{on}. This will allow consistent comparison of proposed transistorized reversible logic systems, specifically addressing situations where some parameters are left out or they are combined improperly.

MODEL

Say the power-clock supply sends energy E_1 to a reversible chip. The chip dissipates fraction $2RC/\tau$, returning fraction $G_L = 1 - 2RC/\tau$ to the power supply.

Thus, G_L is defined as the fraction of the power-clock energy that the reversible logic chip does not turn into heat, instead returning it to the power supply. G_L is a sub unity gain factor.

G_P is defined as the fraction of the power-clock energy returned to the power supply that can be successfully recycled, leading to an additional fraction $G_L G_P$ being sent to the reversible chip.

Thus, G_P is defined as the energy recycling efficiency of the power supply. G_P is also a sub unity gain factor.

This process will repeat, so the chip receives not only E_1, but additional energy that has been recycled one or more times, eventually receiving

$$S = E_1 (1 + G_L G_P + G_L^2 G_P^2 + \ldots),$$

which is a series that sums to

$$S = E_1 / (1 - G_L G_P) = \tfrac{1}{2} C V^2.$$

Thus, S is the "portion" of the original energy E_1 that arrives at the chip, although notably a portion > 1. Since we have not said how much energy was sent in the first place, the equation above defines E_1 based on the reversible chip having received $\tfrac{1}{2} C V^2$, or the energy necessary to charge a signal node.

COMPARISON TO CMOS

Let us now compute the R_{FOM} as the energy of a CMOS circuit divided by the energy of a reversible circuit. We will assume the same transistors are in both circuits. We will also assume that there are the same number of transistors and that average R and C parameters will be the same between CMOS and reversible circuits. The latter assumptions will be approximately correct, yet there is room for debate.

This section will compute R_{FOM} starting with E_C/E_R. E_C/E_R is the CMOS (C) total energy divided by the reversible (R) total energy.

From above, E_1 is

$$E_1 = S (1 - G_L G_P),$$

so let us define E_2 to be energy consumed by the cryocooler,

$$E_2 = S (1 - G_L) P_S,$$

where P_S is the wall-plug energy required to remove one unit of heat. P_S will depend on the temperature, but this document will never need to reference the temperature directly. As stated previously, use $P_S = 0$ for a room-temperature computing system.

The total energy drawn from the wall plug to charge a reversible signal node is,

$$E_R = E_1 + E_2 = S\,((1 - G_L G_P) + (1 - G_L)P_S).$$

Let us define E_3 to be energy dissipated by CMOS,

$$E_3 = S,$$

and E_4 for the cryocooler,

$$E_4 = S\,P_S,$$

for a total E_C of

$$E_C = S\,(1 + P_S).$$

Hence,

$$E_R/E_C = S\,((1 - G_L G_P) + (1 - G_L)\;P_S) \,/\, S\,(1 + P_S)$$

$$= ((1 - G_L G_P) + (1 - G_L)\;P_S) \,/\, (1 + P_S),$$

which after some algebraic rearrangement yields

$$E_R/E_C = 1 - G_L(G_P + P_S)/(1 + P_S)$$

The readers attention is called to the term $(G_P + P_S)/(1 + P_S)$. If $P_S = 0$, the term is equal to G_P, but if $P_S = \infty$, the term is equal to 1. So, P_S is a “control knob” that causes to G_P to disappear.

R_{FOM} AND SUMMARY

Repeating the definitions:

P_S is the specific power, or cooling overhead, of the cryocooler, with $P_S = 0$ if there is no cryocooler.

G_L is the portion of the power-clock energy that the reversible chip does not turn into heat, but returns to the power supply.

G_P is the energy recycling efficiency of the power supply.

I_{off} and I_{on} are the on and off current of a typical transistor.

We will now compute R_{FOM}, yet the most concise formulation computes the max of the lowest energies and then inverts the result, which is

$$R_{FOM} = \max\left(1 - G_L \frac{G_P + P_S}{1 + P_S}, \frac{I_{off}}{I_{on}}\right)^{-1}$$

- If $P_S = 0$, indicating room temperature operation, $E_R/E_C = 1 - G_L G_P$, showing that the energy efficiency improvement of the reversible circuit is in series with the energy recycling of the power supply. It is possible to trade off G_L for G_P, but neither factor can exceed 1. This highlights the importance of considering both the energy efficiency of a reversible chip and energy recycling power supply together.
- If $P_S = \infty$, the limit of cryo operation, $E_R/E_C = 1 - G_L$, showing that a cryocooler can substitute for the energy recycling power supply. A cryocooled reversible implementation may be more energy efficient than a cryo CMOS implementation, but both are likely to be less efficient than a pure room temperature implementation. Thus, cryo operation is most likely to be valuable when there is an external problem constraint requiring computing at a specific temperature, such as quantum computing.
- If $G_P = 0$, indicating no energy recycling power supply, $E_R/E_C = 1 - G_L P_S /(1 + P_S)$, which suggests that $G_L \approx P_S/(1 + P_S)$. In other words, a 1,000× energy efficiency improvement may be possible for 4 K operation where the cooling overhead is typically P_S = 1,000 W/W, but such a boost would not be possible at 77 K because P_S will be too small. So, a large G_L can be spoiled by a small P_S.