Minimizing classical control resources

QRE2022
June 18, 2022

Erik P. DeBenedictis
Zettaflops, LLC

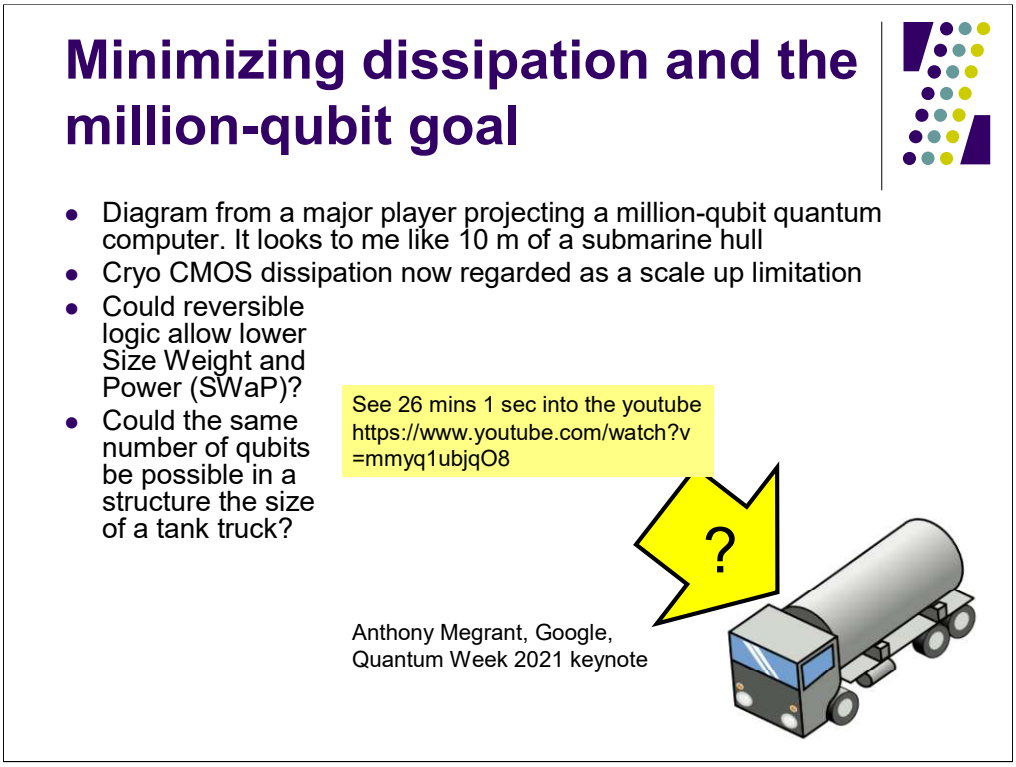


Diagram from Anthony Megrant, Google, Quantum Week 2021 keynote.

Scaling up quantum computers is a widespread priority. Let us consider a goal of a million qubits.

Currently, each of the million qubits will require a special analog control waveform. If the electronics that creates each waveform is located at room temperature, a million microwave transmission lines will need to cross the cryostat boundary. This would be unwieldy and unscalable.

On the other hand, if the control pulses are generated in the cryostat using cryo CMOS, the large energy of the CMOS will require a large cryostat for heat transfer and a high-capacity cryocooler.

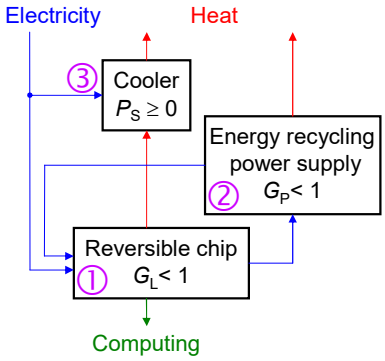
A cryogenic classical logic technology that was more power efficient than cryo CMOS would help.

The diagram includes a cartoon of current plans, which look like 10 m of a submarine, but perhaps a more power efficient cryo technology could reduce system size, weight, and power (SWaP) to the size of a tank truck. Alternatively, the size could stay the same but the structure would have more qubits.

Reversible logic reformulated for cryo, summary

- Chips ① developed in 1990s are pretty good demonstrations of reversible logic
- However, the original reversible logic depended on an unmanufacturable component ②
- With knowledge of quantum computer scaling, reversible logic could be reformulated to replace ② with a cryocooler ③

- Energy/heat flow diagram



- Detail in backup slides

G_P = the energy recycling efficiency of the power supply
$G_L = 1 - 2RC/\tau$, the portion energy not turned into heat
P_S = the cooling over head of the cryo cooler, or 0 if not present (P_S stands for "specific power")

There was a conference in 1981 attended by Feynman, Toffoli, and Fredkin where both quantum and classical reversible computing debuted. This is why we have Toffoli and Fredkin gates in both fields and the CNOT gate is sometimes called the Feynman gate.

Classical reversible logic was studied in the 1990s under DARPA funding (in the USA) and resulted in perfectly satisfactory chips ①, but a second component of the powertrain, the energy recycling power supply ②, was unmanufacturable and caused the field to stall.

It became apparent how quantum computers would scale around 2018. With this information, it was possible to reformulate the reversible logic powertrain so that a cryocooler ③ fills the role unsatisfactorily filled by the energy recycling power supply.

This talk is about the reversible logic as reformulated for cryo.

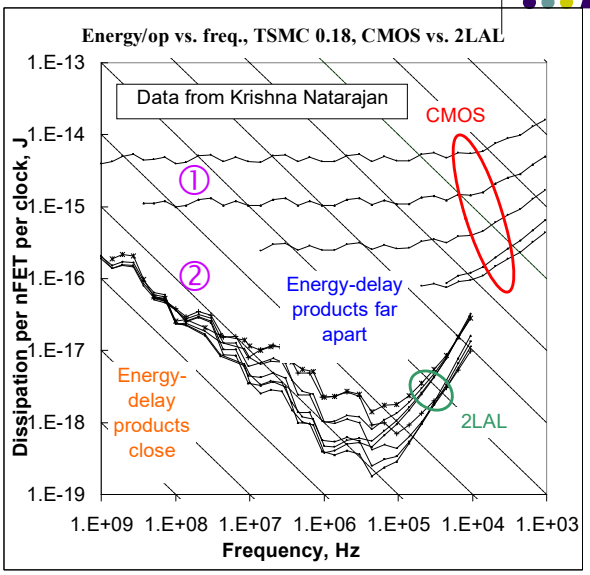
More data in the backup slides.

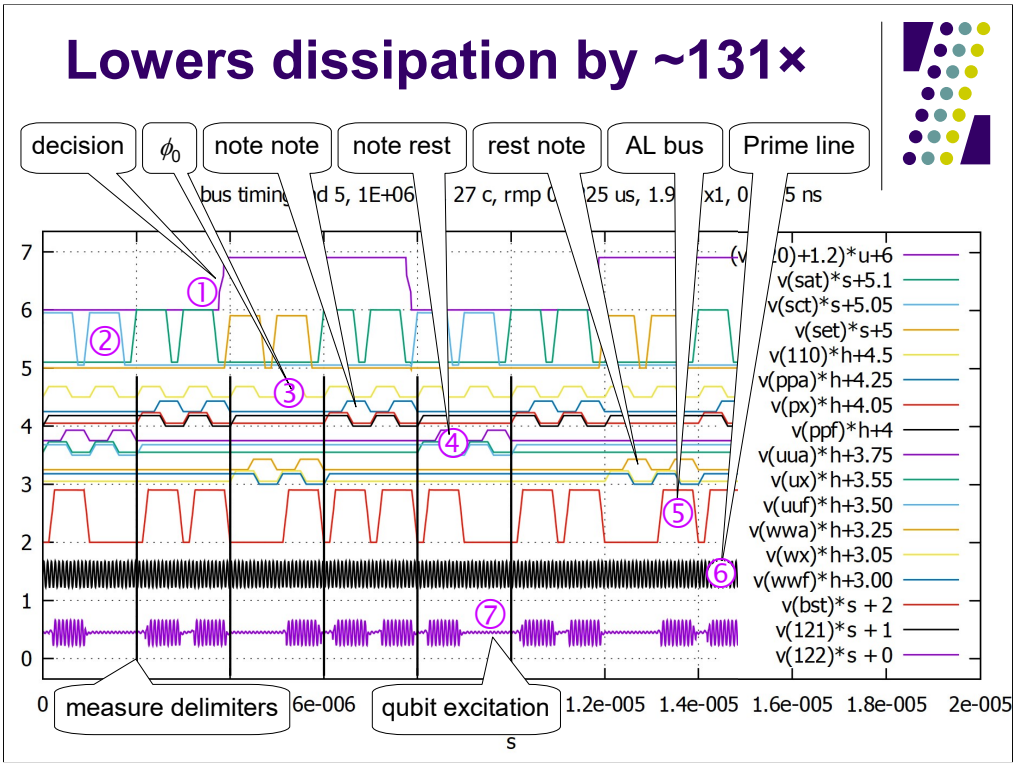
Outline

- The speaker devised a reversible logic controller (RL controller) design
  - Schematic + spice simulation
  - Plan to use in real quantum computers, but …
  - used as an “existence proof” in this talk
- Existence proof of what?
  - No irreversible gates required in cryostat
  - Transistors required in cryostat $\propto$ source code size (no ∞ stack)
  - Universal architecture in cryostat (.gif/.zip decompressor)
  - Other conclusions in backup material
- Natural metric
  - Irreversible gate-ops + reversible gate-ops + total memory, per quantum operation

Can we make the RL controller with reversible shift registers?

- CMOS ① constant energy/op
- Adiabatic energy per op ② drops with clock period
- Qubit measurement about 1,000× slower than CMOS
- Reversible shift registers have been measured with 10-1,000× lower dissipation than CMOS using the same transistors





The diagram shows a reversible logic controller (RL controller), which is in turn part of the PL/AL architecture. The RL controller becomes an existence proof that lower dissipation is possible. A schematic diagram (see 2nd subsequent slide) can be simulated. The simulation shows functional correctness and some information on dissipation.

The overall project included comparing simulated dissipation of the RL controller and a cryo CMOS work alike. This showed a 131× decrease in dissipation.

① Decision line from standard computer at room temperature. When the gate operation sequence reaches a branch point, this signal must be stable at a 0 or 1.

② These are basically state bits that say which of three musical measures are active at a given instant, the three signals are each a different color and overlaid.

③ Phase 0 clock.

④ Three signals of the data controlled clock for the “note note” music. Note that the lower two lines are the same phase, but stop at a different point. This identifies one of them as the bus enable clock.

⑤ This is the true data wire of the address-line bus, equivalent to the inverse position of the pianist’s finger. The bus driver is different for each measure of music, with the signals being note-rest-note-note-rest-note.

⑥ Prime line, which is a sine wave for simulation.

⑦ Modulated wave to the qubits.

Process: Algorithm-flowchart-schematic-fab

- Error correction procedure

1. Use the circuit of Fig. 2(c) to extract the *XZZXI* syndrome. ①

   (a) If the flag qubit is measured as |->, then use the unflagged circuits analogous to Fig. 2(b) to extract all four syndromes. Finish by applying the corresponding correction from among *IIIII*, *IIZXI*, *IXZXI*,*IYZXI*, *IZZXI*, *IIIXI*, *IIXXI*, *IIYXI*.

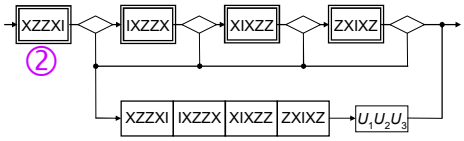
   (b) Otherwise, if the syndrome is −1, i.e., the syndrome qubit is measured as |1>, then use unflagged circuits to extract all four syndromes. Finish by applying the corresponding correction of weight ≤ 1.

2. (If the flag was not raised and the syndrome was trivial, then) Similarly extract the IXZZX syndrome. If the flag is raised, then use unflagged circuits to extract the four syndromes, and finish by applying the correction from among *IIIII*, *IIIIX*, *IXXII*, *IIIXX*, *XIIIY*, *IXIII*, *IIIZX*, *IIIYX*…

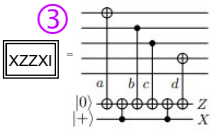
From: Chao, Rui, et. al "Quantum error correction with only two extra qubits." Physical review letters 121.5 (2018): 050502.

- Create "flowchart"

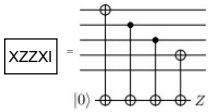
[[5, 1, 3]] error detection and correction with flags:



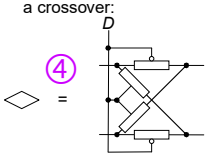
Circuit with flag qubits:



Circuit without flags:



Decision, implemented by a crossover:



Correction:

= Z, Y, or Z on qubit *n*

Background: The Prime-line/Address-line (PL/AL) architecture uses "prime" microwave waveforms created at room temperature for gate operations. These waveforms are distributed to all qubits to be keyed on and off by a control system "pianist." The pianist uses something like music ③ to create the pattern, but a room temperature control computer directs higher level activities like a "playlist" and repeats.

① an example algorithm, specifically quantum error detection and correction for [[5, 1, 3]] code. Task is to apply stimulus to qubits, such as 1 or 2 qubit operations, resets, and measurements.

② the algorithm can be represented by a flowchart, where the boxes represent a quantum gate sequences ③ and the diamonds are decisions ④.

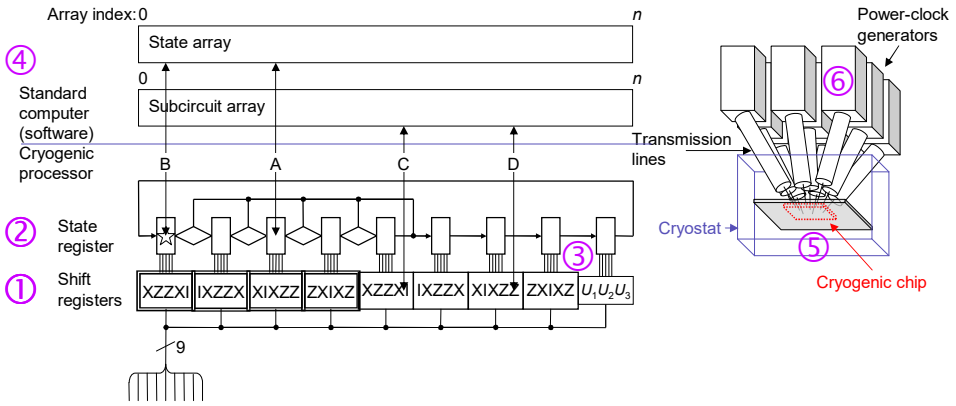
•Flowchart boxes contain a label (XZZXI) to identify a subcircuit sequence. These sequences are like measures in music in that they can only be of a limited length due the need for error correction cycles.

•Decisions are provided by a separate subsystem at room-temperature.

•The correction unit $U_1U_2U_3$ is a detail not fully described in this slide deck.

Hybrid computing system

- Yields an integrated multi-temperature computing system
  - Function
  - Powertrain
- Only reversible shift registers at cryo stage
- If you think about it, cryo stage is a zip/gif decompressor



The diagram shows a linearized version of the flowchart and its connection to a room temperature computer.

The shift registers with music ① are in a row.

The state registers ② represent the state of the flowchart with a 1 bit, which advances to the right or jumps due to diamonds.

The state machine turns the music on an off via data-controlled clocks ③, one of which is relayed to an “address-line bus” that controls qubits.

A room temperature computer shadows the state of the reversible logic in arrays ④ and uses software to control the diamonds of the flowchart.

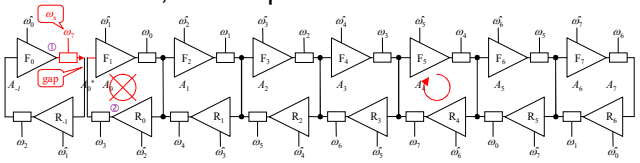
On the right:

The reversible computing system also includes a cryo-adiabatic powertrain, comprising a cryogenic chip ⑥, room temperature power-clock generators ⑤, and transmission lines into the cryostat.

Backup: Data-controlled clock and bus circuits for the boxes

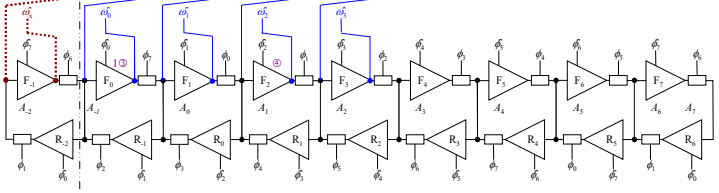
- Substitute these circuits, but keep flowchart interconnect as wires

①



- Substitute crossover for diamonds (previous slide)
- Fab a chip

②



Ngspice simulation code on the Web rigorously defines the circuits.

Circuit ① is a reversible shift register using a static, even-load circuit called Q2LAL. The red annotations allow driving a bus reversibly.

Circuit ② is a data-controlled clock. Adorning the state shift register with the extra circuitry on top creates a clock that runs while the input is a 1. If the input bit is a 0, the clock stops systematically. With the red annotations in ①, some shift register outputs to “tri state.”

Each diamond is replaced by a crossover (④ on the second previous slide). An external computer controls the crossover.

Note: There is an optimization that involves a CNOT gate.

Existence proofs of what? This is what…

- No irreversible gates needed in cryostat
- Number of gates required in the cryostat is proportional to the length of source code rather then depth of recursion stack
- Circuit in cryostat is like a .gif/.zip decompressor

- More interesting results in backup material

Some additional detail:

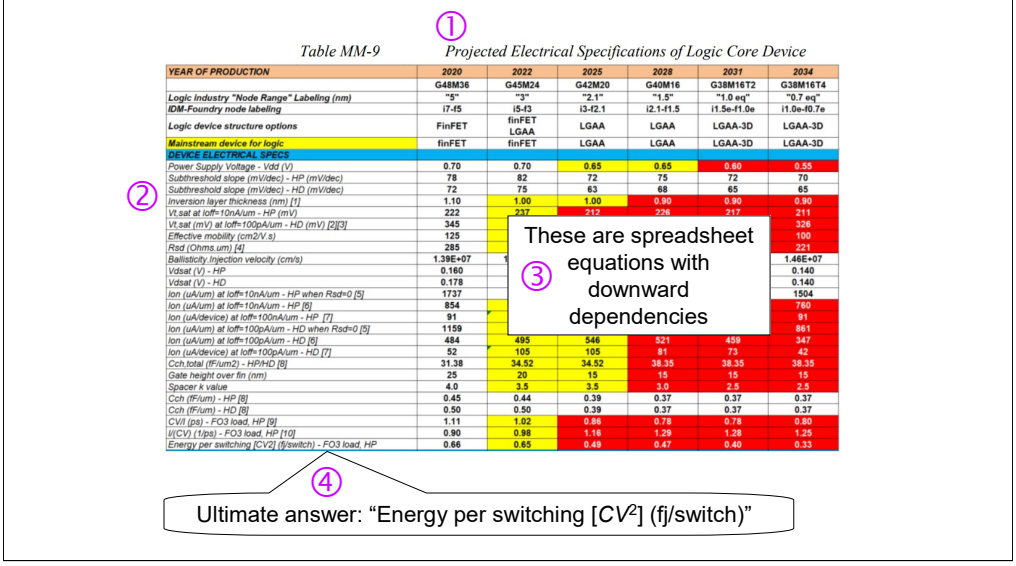
First bullet: The design process created the cryogenic part of the control system entirely from reversible gates, so apparently no irreversible gates are required.

Caveats: (a) I have a optimization that uses some CNOT gates. (b) Diamonds are effectively externally controlled Fredkin gates. (c) Irreversible gates may be needed during boot-up.

Second bullet: The design process created the cryogenic part by substituting schematic diagrams for programmatic constructs. This cannot result in a component more than a constant factor larger than the program text (such as an arbitrarily large pushdown stack). (The pushdown stack is at room temperature.)

Third bullet: The in-cryostat component is essentially a .gif/.zip decompressor.

Resource estimation I adapt ITRS/IRDS format



① *Table MM-9 Projected Electrical Specifications of Logic Core Device*

YEAR OF PRODUCTION	2020	2022	2025	2028	2031	2034
	G48M36	G45M24	G42M20	G40M16	G38M16T2	G38M16T4
Logic industry "Node Range" Labeling (nm)	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i7-i5	i5-i3	i3-i2.1	i2.1-i1.5	i1.5e-i1.0e	i1.0e-i0.7e
Logic device structure options	FinFET	finFET LGAA	LGAA	LGAA	LGAA-3D	LGAA-3D
Mainstream device for logic	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
DEVICE ELECTRICAL SPECS						
Power Supply Voltage - Vdd (V)	0.70	0.70	0.65	0.65	0.60	0.55
Subthreshold slope (mV/dec) - HP (mV/dec)	78	82	72	75	72	70
Subthreshold slope (mV/dec) - HD (mV/dec)	72	75	63	68	65	65
Inversion layer thickness (nm) [1]	1.10	1.00	1.00	0.90	0.90	0.90
Vt.sat at Ioff=10nA/um - HP (mV)	222	237	212	226	217	211
Vt.sat (mV) at Ioff=100pA/um - HD (mV) [2][3]	345					326
Effective mobility (cm2/V.s)	125					100
Rsd (Ohms.um) [4]	285					221
Ballisticity,Injection velocity (cm/s)	1.39E+07					1.46E+07
Vdsat (V) - HP	0.160					0.140
Vdsat (V) - HD	0.178					0.140
Ion (uA/um) at Ioff=10nA/um - HP when Rsd=0 [5]	1737					1504
Ion (uA/um) at Ioff=10nA/um - HP [6]	854					760
Ion (uA/device) at Ioff=100nA/um - HP [7]	91					91
Ion (uA/um) at Ioff=100pA/um - HD when Rsd=0 [5]	1159					861
Ion (uA/um) at Ioff=100pA/um - HD [6]	484	495	546	521	459	347
Ion (uA/device) at Ioff=100pA/um - HD [7]	52	105	105	81	73	42
Cch,total (fF/um2) - HP/HD [8]	31.38	34.52	34.52	38.35	38.35	38.35
Gate height over fin (nm)	25	20	15	15	15	15
Spacer k value	4.0	3.5	3.5	3.0	2.5	2.5
Cch (fF/um) - HP [8]	0.45	0.44	0.39	0.37	0.37	0.37
Cch (fF/um) - HD [8]	0.50	0.50	0.39	0.37	0.37	0.37
CVit (ps) - FO3 load, HP [9]	1.11	1.02	0.86	0.78	0.78	0.80
Ii(CV) (1/ps) - FO3 load, HP [10]	0.90	0.98	1.16	1.29	1.28	1.25
Energy per switching [CV2] (fj/switch) - FO3 load, HP	0.66	0.65	0.49	0.47	0.40	0.33

②

③ These are spreadsheet equations with downward dependencies

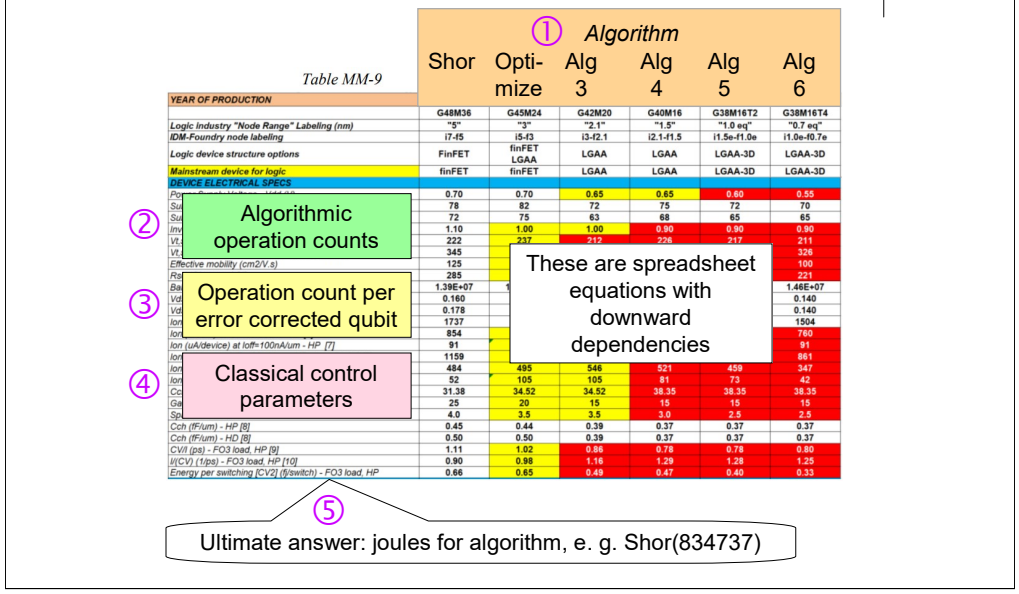
④ Ultimate answer: "Energy per switching [CV^2] (fj/switch)"

The International Technology Roadmap for Semiconductors (ITRS), now the International Roadmap for Devices and Systems (IRDS) may provide an example of how to organize resource estimation.

The iconic colored charts are an Excel spreadsheet. Each column represents a year and is filled with a series of constants and equations with top-to-bottom dependency. The equations compute switching energy for CMOS based on Moore's law assumptions.

Quantum resource estimation is not Moore's law, but perhaps other aspects of the chart are useful.

Resource estimation II: quantum algorithm w/control



① The columns are renamed to be algorithms, such as Shor, optimize, etc.

② Existing quantum resource estimation yields functions for, say, the number of Toffoli magic states required to factor number *N*. These equations are put into cells to the right of the box.

③ Attention today is focused on logical qubits. This area represents the number of single-qubit resources required for, say, a Toffoli magic state.

④ The section to the right of the box includes equations for the number of (ir)reversible gate-ops and total bits (i. e. memory) for each quantum op above.

⑤ The spreadsheet performs the multiplies and adds to compute, for example, the total power and total chip area for the algorithm illustrated based as a function of *N*.

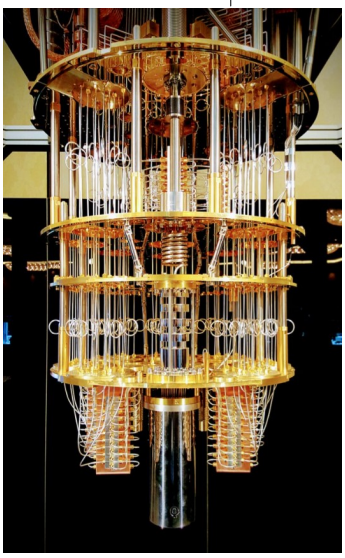
Conclusions

- Resource model builds on Landauer's minimum dissipation and physics of computation rather than commercial products (e. g. ST Micro 28 nm, 22FFL)
- Developed RL controller out of 100% reversible shift registers
- Simulations suggest >100× dissipation reduction over a cryo CMOS work-alike (but there are many undetermined factors)
- Can prove various things using RL controller as an existence proof:
  - No irreversible gates needed in cryostat
  - Resources in cryostat are proportional to source code length
  - Universal cryostat architecture (like .gif/.zip controller)

- Additional data at https://zettaflops.org/qre-2022

Problem description

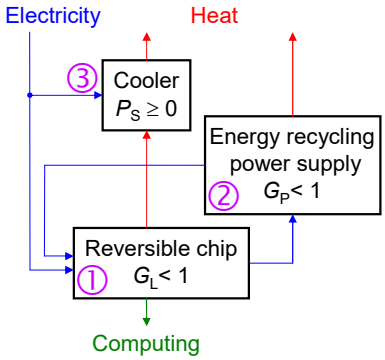
- Quantum computers are a national priority
- The structure on the right does not scale
- For cryogenic qubits, the accepted direction is to compress the data in the cables and use cryogenic electronics to decompress
- *De facto* cryo electronics is cryo CMOS at 4 K, which works about the same as 300 K
- CMOS improving at 2×/decade due to fab, which is not enough for the national priority
- Can we do better?
- Photo by Lars Plougmann, https://www.flickr.com/photos/criminalintent/39660636671, license https://creativecommons.org/licenses/by-sa/2.0/



The adiabatic powertrain

- At room temperature, loop ① and ② recycle energy
- At 4 K, cryocooler overhead $P_S \approx$ 1,000, so recycling is no better than avoiding the cryocooler
  - Let ② be a resistor at room temperature $G_P = 0$
- R_{FOM}, Reversible Figure of Merit (FOM),
  - $R_{FOM} = E_{CMOS}/E_{Reversible}$ ④

- Three variable structure



P_S = the cooling overhead of the cryocooler, or 0 if not present (P_S stands for "specific power")
$G_L = 1 - 2RC/\tau$, the portion energy not turned into heat
G_P = the cooling over head of the cryocooler, or 0 if not present
I_{on}/I_{off} is the on/off currents of typical transistors

Ref: Erik DeBenedictis, *Figure of Merit for Reversible Logic Systems*. Zettaflops, LLC technical report ZF011, https://zettaflops.org/wolte-2022/.

The next three slides expand on an argument in Erik DeBenedictis, *Figure of Merit for Reversible Logic Systems*. Zettaflops, LLC technical report ZF011 v1, https://zettaflops.org/wolte-2022/.

The next three slides show why room temperature reversible logic could not be productized, but cryogenic reversible logic is different. This diagram applies to room temperature reversible logic if $P_S = 0$ and cold reversible logic if $P_S > 0$. $P_S \approx 1{,}000$ for cooling to 4 K.

At room temperature, reversible logic recycles wall-plug energy many times through ① and ② for an efficiency increase of ~1,000×. The cryocooler in a quantum computer ③ has an overhead of $P_S \approx 1{,}000$, so an approach that routes energy so it does not go through the cryocooler could give the same benefit.

Energy exits reversible chip ① via two paths, ② (which does not go through the cryocooler) and ③, which is the cryocooler. The approach is to replace the energy recycling power supply with a resistor at room temperature.

In a quantum computer, the objective is to save energy over cryo CMOS, which can be expressed as maximizing a figure of merit $R_{FOM} = E_{CMOS}/E_{Reversible}$ ④.

For offline reading:

P_S is "specific power," or the number of watts that must be provided to a cooling system to remove one watt from a cooled environment.

G_L is the sub unity power gain of a reversible chip, G_L has been demonstrated to about 99.9%

G_P is the sub unity power gain of the energy recycling power supply, G_P has been demonstrated to about 95%.

R_{FOM} at room temperature

- Reversible Figure of Merit (R_{FOM}) = $E_{reversible}/E_{CMOS}$ with no cryostat

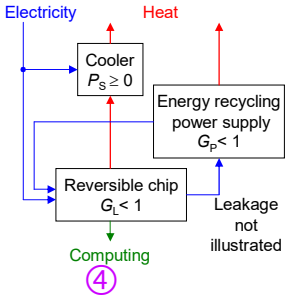
Start with

$$R_{FOM} \overset{①}{=} (1 - G_L \frac{G_P \overset{②}{+} P_S}{1 + P_S})^{-1}$$

If $P_S = 0$ (heat sink),

$$R_{FOM} = (1 - G_L \overset{③}{G_P})^{-1}$$

For reference:



- This is the traditional approach

P_S = the cooling overhead of the cryocooler, or 0 if not present (P_S stands for "specific power")
$G_L = 1 - 2RC/\tau$, the portion energy not turned into heat
G_P = the cooling over head of the cryo cooler, or 0 if not present
I_{on}/I_{off} is the on/off currents of typical transistors

Let us consider room temperature operation where $P_S = 0$.

R_{FOM} ① is CMOS energy divided by reversible circuit energy. Equation ① is not very hard to work out, but the derivation is not in this slide deck.

R_{FOM} has a term ② that degenerates into familiar forms based on P_S.

Substituting $P_S = 0$ would be correct for a room temperature system cooled by a heat sink. Simple algebra yields $R_{FOM} = 1/(1 - G_L G_P)$ ②, as expected. This is the recycling equation that has governed the field for decades ④.

For room temperature operation, the only thing that is important is the product by $G_L G_P$, which is why all slide decks and papers have two sections, one for G_L, the chip's efficiency (which is touted), and G_P, the recycling efficiency (which is not as good). As a result, reversible logic has been presented as a long-term research direction.

R_{FOM} at 4 K

- Reversible Figure of Merit (R_{FOM}) = $E_{reversible}/E_{CMOS}$ with cryostat

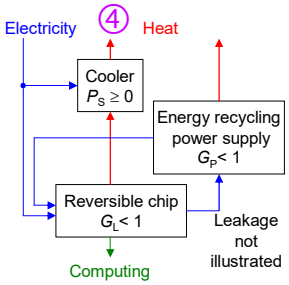
Start with

$$R_{FOM} = (1 - G_L \frac{G_P + P_S}{1 + P_S})^{-1}$$ ②

As P_S goes from 0→∞, ①
$(G_P + P_S)/(1 + P_S)$ goes from G_P to 1

$$R_{FOM} = (1 - G_L)^{-1}$$ ③

For reference:



- Chip demos 1995-2008 validated G_L, which is what quantum needs!

P_S = the cooling overhead of the cryocooler, or 0 if not present (P_S stands for "specific power")
$G_L = 1 - 2RC/\tau$, the portion energy not turned into heat
G_P = the cooling over head of the cryo cooler, or 0 if not present
I_{on}/I_{off} is the on/off currents of typical transistors

As the temperature of the reversible chip goes down, the cooling overhead P_S goes up. 4 K is often used as a baseline for quantum computer electronics, where $P_S \approx$ 1,000. However, $P_S = \infty$ leads to the same conclusions for this slide deck, so we will use this value. Substituting $P_S = \infty$ will cause the problematic term G_P from the previous slide to "disappear" ③. Explanation:

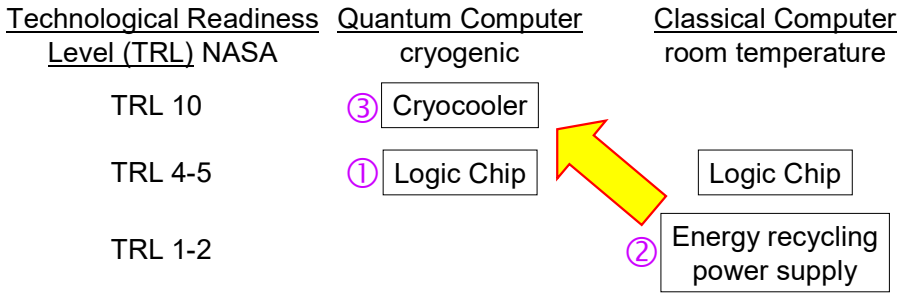
If P_S is very large ①, $G_P + P_S \approx P_S$ and $1 + P_S \approx P_S$, so R_{FOM} ② becomes $(1 - G_L)^{-1}$ ③, which his like erasing the problematic term G_P from the last slide.

Interestingly, the demo chips built in the 1994-2008 demonstrated the key checkpoint for reversible logic quantum computer control – but the experimenters did not know this at the time because quantum computers were not well enough defined to know the requirements for the cryogenic classical logic.

Additional detail: P_S does not become infinite in a quantum computer, but is about 1,000 at 4 K. However, the "crossover point" is where P_S is about equal to the slowdown factor. The slowdown factor in a quantum computer is about the ratio of CMOS speed to quantum measurement speed, which is about 1,000 as well. So we are OK, but close to the limit.

Projects with fewer big risks are more likely to be funded

- A reversible computing system needs a chip and an energy management component
  - Room temperature reversible computing uses an energy recycling power supply—proposed based on resonators, MEMs, and switching circuits
  - If a cryocooler is already present, it will fill the same role
- Reduces risk; suggests two-stage plan



The cryo-reversible powertrain needs two parts, a reversible logic chip ① and an energy handling unit ② or ③.

Extending the energy efficiency of a (room-temperature) reversible microprocessor chip to the wall plug would require an energy recycling power supply ②. Energy recycling power supplies are at at a lower TRL level (see note) than reversible chips, so this would link two research projects to one another, increasing risk.

However, a cryogenic reversible logic quantum control chip would naturally use a cryocooler for the same function. A cryocooler is TRL 10, an off-the-shelf item.

TRL level is “Technology Readiness Level,” a NASA term. See https://en.wikipedia.org/wiki/Technology_readiness_level

Thus, there less risk for a cryogenic reversible system.

Existence proofs of what? This is what…

No irreversible gates required in cryostat

- Landauer's minimum is "order of *kT* per irreversible function"
- RL controller has no irreversible gates
- Cryo CMOS design tools lay out mostly irreversible gates
- Caveats: One of my papers has a CNOT for optimization; crossover is an externally controlled Fredkin gate; have data-controlled clocks

Reversible circuit is of bounded and reasonable size

- Reversible gate dissipation = $(2\ RC/\tau) \times (\frac{1}{2}CV^2)$
- For 1 μs quantum measurement, $(2\ RC/\tau) \approx 1/1{,}000$
- Bennett showed all-reversible computers are possible, but with overhead [Bennett]
- By construction, RL Controller has no infinite stack and data in shift register proportional to source code size

The RL controller circuits forms an existence proof, but of what? It is an existence proof that no irreversible gates are needed in the cryostat.

(right) Landauer identified a minimum dissipation for an irreversible gate, but the minimum does not apply to reversible gates. If the gates are based on transistors, the dissipation is about the same as CMOS at its top clock rate. However, the dissipation decreases linearly with clock period (2 RC/τ).

As stated earlier, qubit measurement is much slower than CMOS, about 1,000× slower.

However, we must address the possibility that reversible logic would require vastly more gates than a CMOS equivalent. This turns out not to be true, as the flowchart will only have a much "music" stored as is in the original algorithms. There is not, for example, a need for a "stack" in the cryostat that contains potentially unbounded storage.

Flowcharts and Turing completeness

- Circuit is like a data decompressor for .gif and .zip files
- Musical measures are “symbols”
- Data stream influences a state machine, steering output of symbols kind of probabilistically based on symbol frequency
- Note: RL controller loads symbols during cryogenic cooldown using irreversible circuits
- Turing complete as a hybrid
- A paper [Böhm 66] showing that a flowchart is only “Turing complete” only if accompanied by a stack
- Righto, the stack is a room temperature and influences a stack-free flowchart through crossovers

[Böhm 66] Böhm, Corrado, and Giuseppe Jacopini. "Flow diagrams, Turing machines and languages with only two formation rules." *Communications of the ACM* 9.5 (1966): 366-371.

Landauer's minimum dissipation in a hybrid system

Physicist vs. computer architect

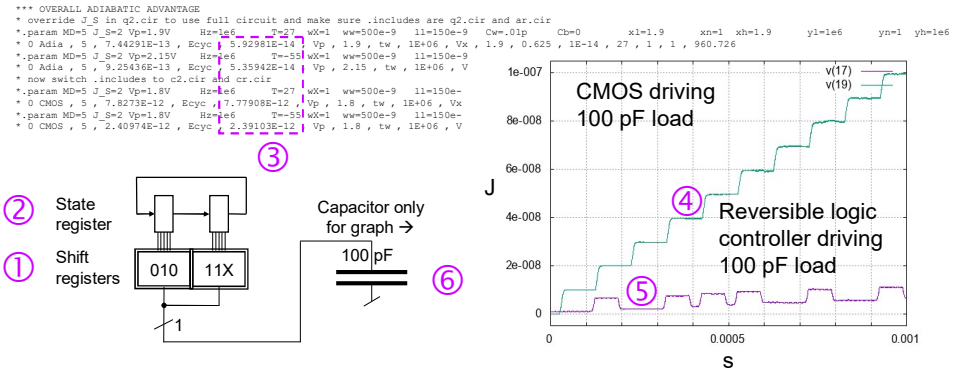
- Landauer's minimum is kT per irreversible operation
- In a mixed temperature environment, which T do we use?
- Physicist's answer: The T of the environment performing the function
- Computer architect's answer: What are the limits of moving the irreversible operations to an environment where T is most favorable?

Proposed hybrid multi-temperature computing architecture

- Room temperature:
  - Compute the output
  - Compress the output
- Cable:
  - Move compressed string into the cryostat
- Cryo electronics:
  - Decompress the output

Results of Simulation

- ngspice Sky130; CMOS from standard cell
  - R_{FOM} 1 MHz 131 @ 27 C
  - Note: Other orgs chips include an instruction set, raising dissipation
- Simulation output:



The ngspice simulation has two data-controlled clocks ② and two registers ① holding 3 notes of “music” each. The “music” is 010 and 11 or 111.

The output of a simulation run is shown above ③. There were four 1 MHz runs in the combinations of CMOS/Adiabatic and 27 C/-55 C. Adiabatic supply voltages were1.9 V (27 C) and 2.05 V (-55 C) and 1.8 V for CMOS. Wire capacitance was .01 pF. The first period of a 20 cycle run has startup effects, so Ecyc is averaged over the remaining 19 cycles.

Within the purple dashed line, $R_{FOM} = E_{CMOS}/E_{Adia}$ yields 131 at 27 C. The -55 C CMOS simulation did not function.

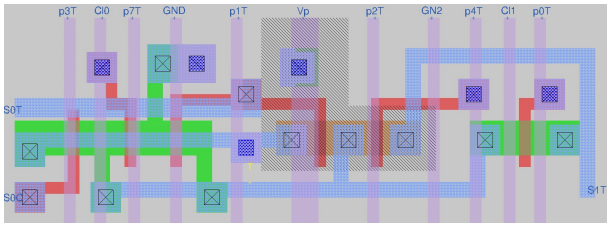
The graph demonstrates functionality from a simulation, with same architecture ① and ②, but with a different transistor model, a 10 V supply, and a 100 pF capacitor ⑥ on the output bus. Curve ④ is a reference for CMOS, which rises by $½CV^2$ each on the rising edge of the clock. Curve ⑤ is the output.

The was an oversight in the original circuit creating the graph: the second music register was only two stages long instead of three. The missing stage made no functional difference because it was initialized to all 1s. The oversight has been fixed, but the graph on the right appeared in some documents, so the original version is used here for comparisons. For what appears below, assume the second music register holds 111.

The music 010 plays first and alternates with 111. The output (5) represents 3 1/3 “musical measures” of these three notes. The pattern is 01<u>0</u> 111 010 1. So (5) is on top of the underlined <u>0</u> in the preceding sequence.

Sky130 validation (in progress)

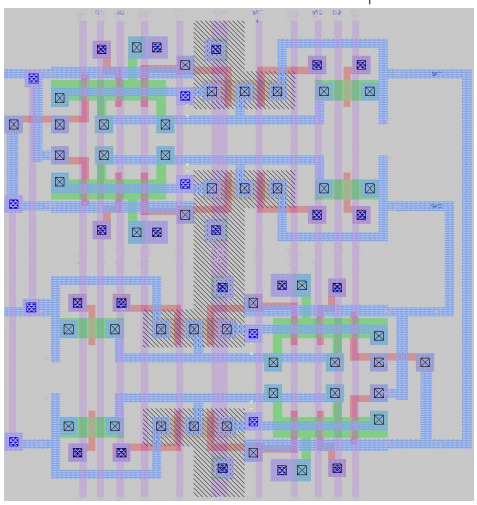
- Sky130 is an “open” PDK for multi-project wafers, based on a 130 nm process (I have no cryo data)
- Activity
  - “Note note” has been hand-coded in ngspice and various simulation results have been presented at conferences
  - The replicable unit of Q2LAL (circuit family) is shown below. It has been extracted with parsitics and can be incrementally substituted into the hand-coded ngspice
  - Results are in line with predictions
    - 131× advantage over Cryo CMOS from Sky130 standard cells



Validation was also performed using Sky130 layout. To assure constraints like even load, the basic replication unit should be create from a single template with reflections and rotations. The reflections and rotations require solving a puzzle on how to organize the flyover wires.

Sky130 full phase

- The cell illustrated is the most common stage
  - Top: The stage
  - 2nd quarter: Vertical flip
  - 3rd quarter: Horizontal flip
  - Bottom: 180° rotation
  - Not optimized
- There are other, less common cells
  - Data-controlled clocks
  - Bus interfaces
  - Crossovers (trivial)



Full stage of Q2LAL. Replication units are flipped v and h and rotated 180°. Not exactly balanced due to the need for crossovers.