On-board Processing Expandable Reconfigurable Architecture (OPERA) Program Overview

Fault-Tolerant
Spaceborne Computing
Employing New Technologies
Workshop

29 May 2008

Michael Malone
Draper Laboratory

OPERA Program Motivation

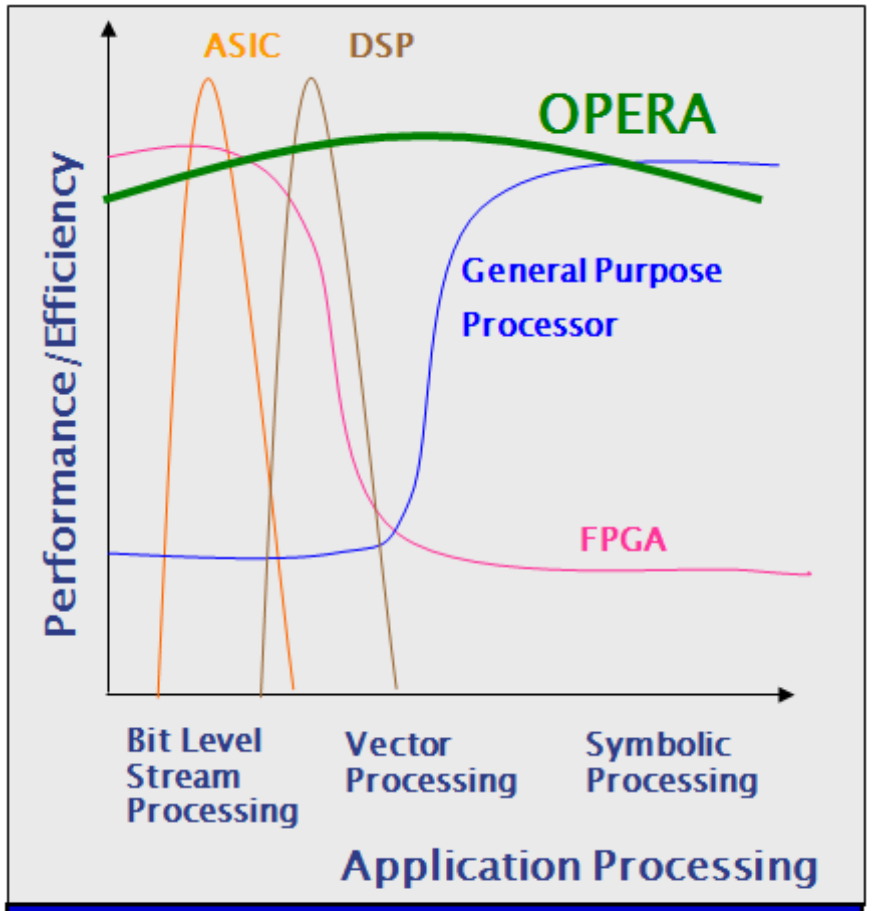
Revolutionary improvement in processor capabilities for space applications

- **Space Processing Challenges**
  - **Advancing mission requirements**
  - **Shrinking decision timelines**
  - **Providing a common high-performance hardware and software technology foundation**

- **OPERA provides processing leap-ahead capability**
  - **Breaks the paradigm of space electronics being 2 or more generations behind the commercial sector**
  - **Produces a radiation hardened state of the art general purpose processor**
    - ***100x more capable than current space qualified devices***

Principle OPERA Components

- **Hardware – MAESTRO Chip**
  - 49 core, 90 nm CMOS
  - 70 GOPS, 10 Gbps throughput
  - Radiation Hard By Design (RHBD)
  - Developed by Boeing SSED
    - Uses Tilera Corporation IP
    - Additional third party IP
- **Software – ISI East**
  - Basic Compiler Tools
  - Parallel Libraries
  - Benchmarks
  - Performance and Productivity Tools
    - Parallel Analysis
    - Parallel Debugger
    - Run Time Monitor



Excellent performance across all processing domains

OPERA Program History

MIT PCA Concept Article

"Baring It All to Software: Raw Machines"
IEEE, September 1997

http://cag.csail.mit.edu/raw/documents/Waingold-Computer-1997.pdf

DARPA PCA Program

http://www.darpa.mil/ipto/Programs/pca/pca.asp

Program Manager:
Dr. William Harrod
1999 - 2006

MIT RAW Processor

Raytheon Monarch Processor

Univ. of Texas - TRIPS

IBM Cell Processor

Graphic Processing Units

?

OPERA PM:
Dagim Seyoum

Government Independent Architecture Analysis - 2006

DARPA PM:
Michael Fritze

DTRA PM:
Lew Cohn

DARPA / DTRA RHBD 2 Program

90 nm RHBD Libraries

Solid-State Electronics Development — SSED — BOEING

Design Files

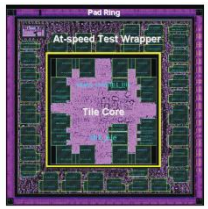
Tilera TLR26480 Processor

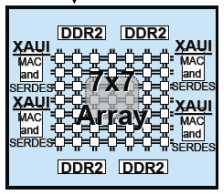
2nd Generation RAW Device, IP Procurement 6/2007

OPERA Software

TAPO

Single RHBD Tile 4/2008



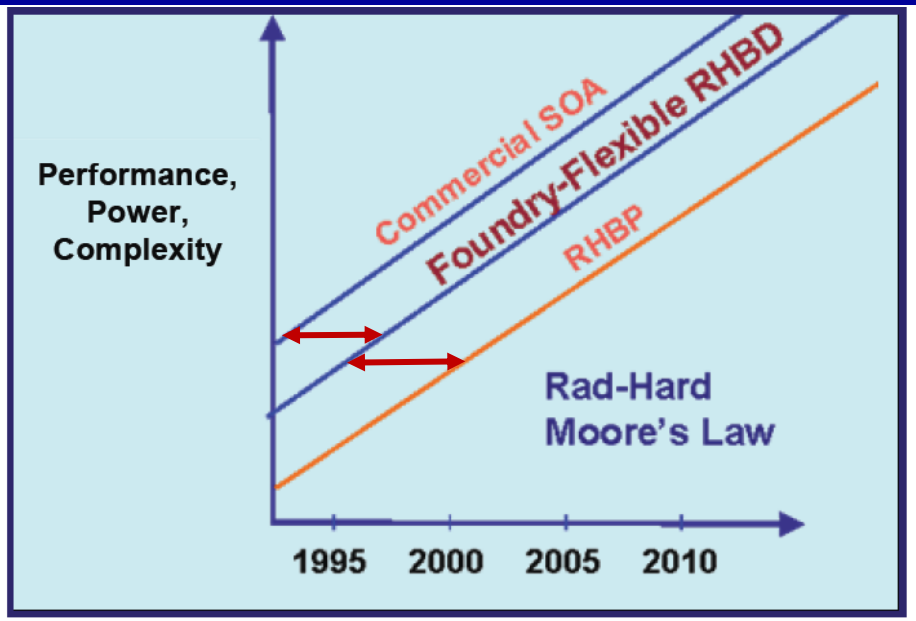


49 Core RHBD TRL 6 Chip 12/2010

Next - Generation Space Computer Board

DARPA / DTRA RHBD 2 Program

- **Enable Rad-Hard ASICs on advanced commercial fab processes**
  - High performance, low power
  - Leverage supported IP & tools
  - Foundry flexible assured sources

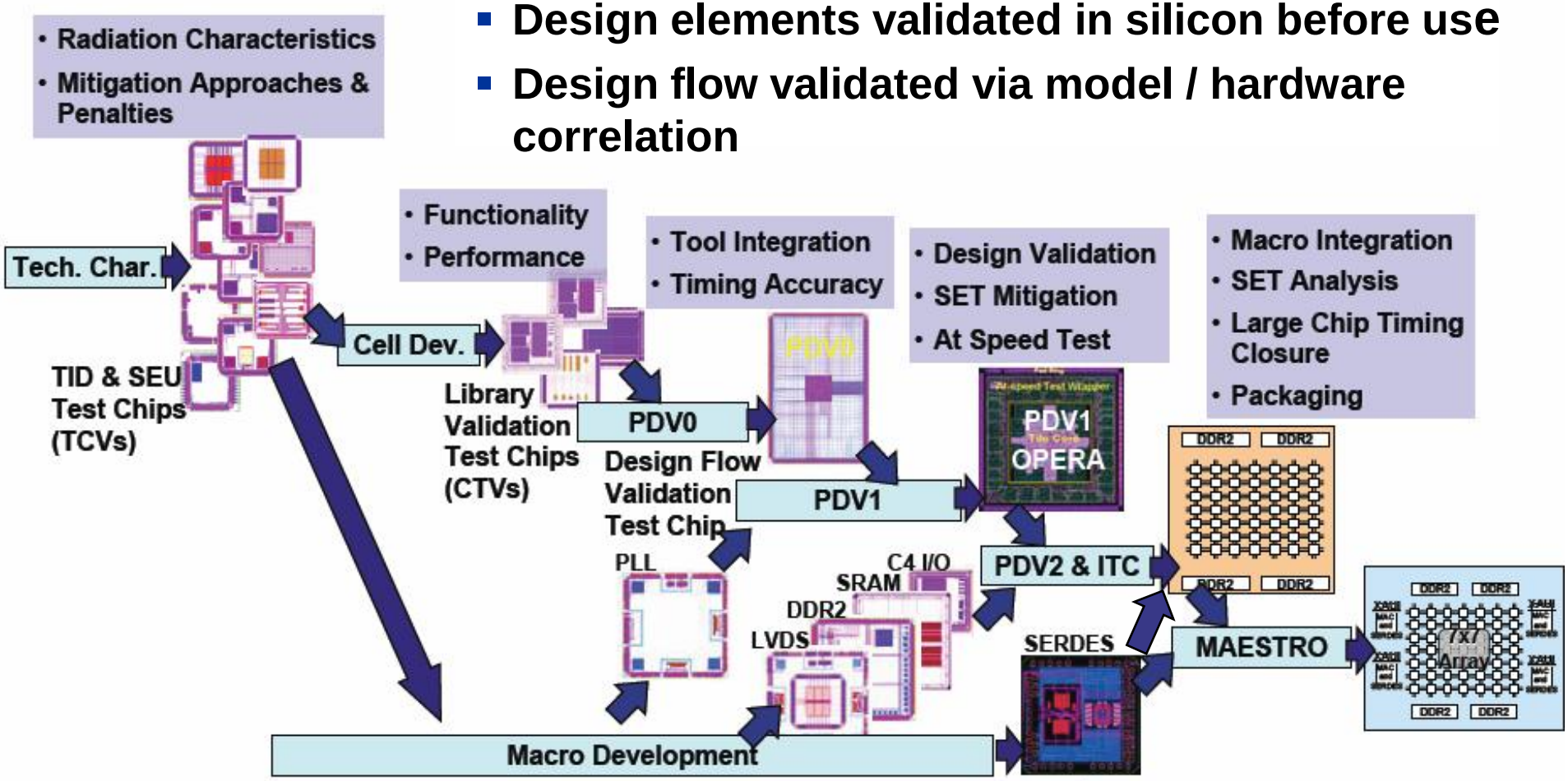


Hardness Targets	
Total Ionizing Dose	> 2 Mrad(Si) (OPERA > 500 Krad(Si))
Single Event Upset	< 1E-10 errors/bit-day (Adams), LET_{Th} > 20
Single Event Latchup	LET_{TH} > 120 Mev-cm^2/mg
Dose-Rate Upset	>1E10 rad(SiO_2)/sec

Acceptable RHBD Penalties	
Area	≤ 2X
Speed	≤ 1.5X
Power	≤ 2X

RHBD Risk Mitigation Approach

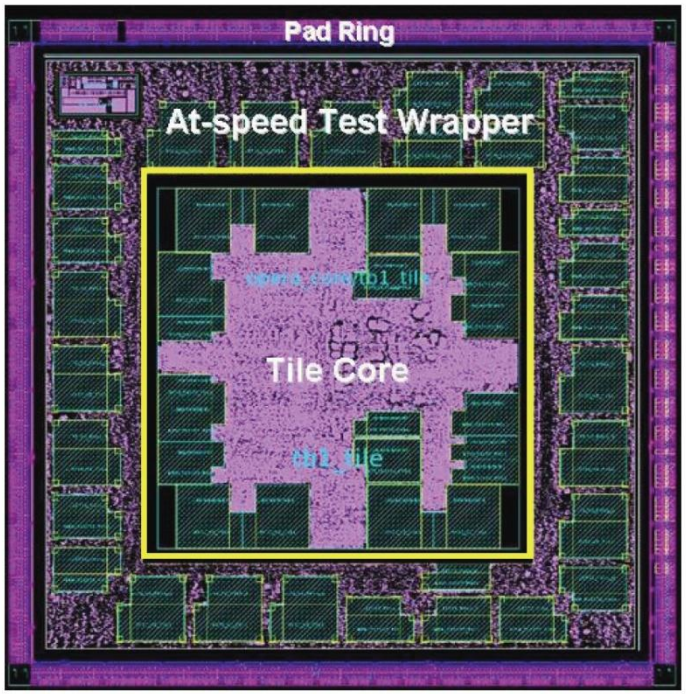
- Design elements validated in silicon before use
- Design flow validated via model / hardware correlation



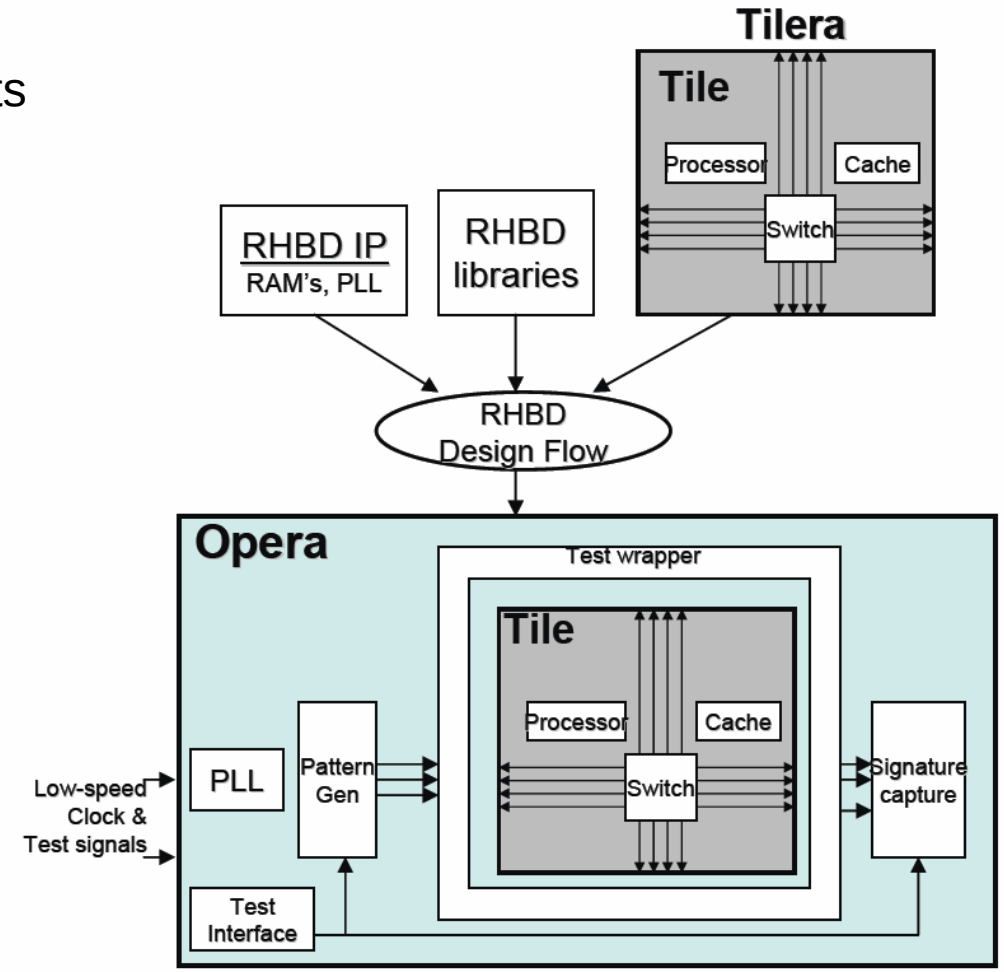
- PDV – Product Demonstration Vehicle
- ITC – Integrated Test Chip

The OPERA RHBD Tile

- **Risk Reduction Effort for MAESTRO**
- **RHBD Program Product Demonstration Vehicle #1**
  - 9 x 9 mm with test wrapper
  - 1.7M Gates, 2.4M Memory Bits
  - 500 I/O Pads

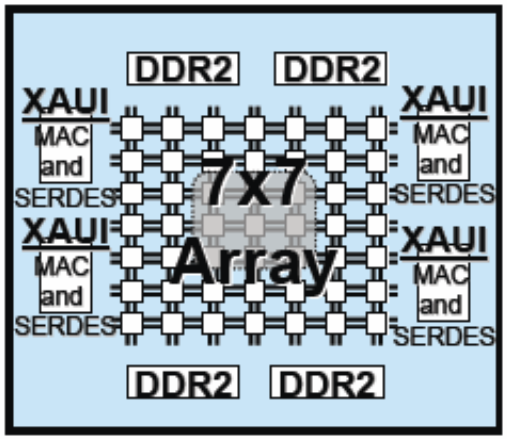


TAPO Tapeout April 2008



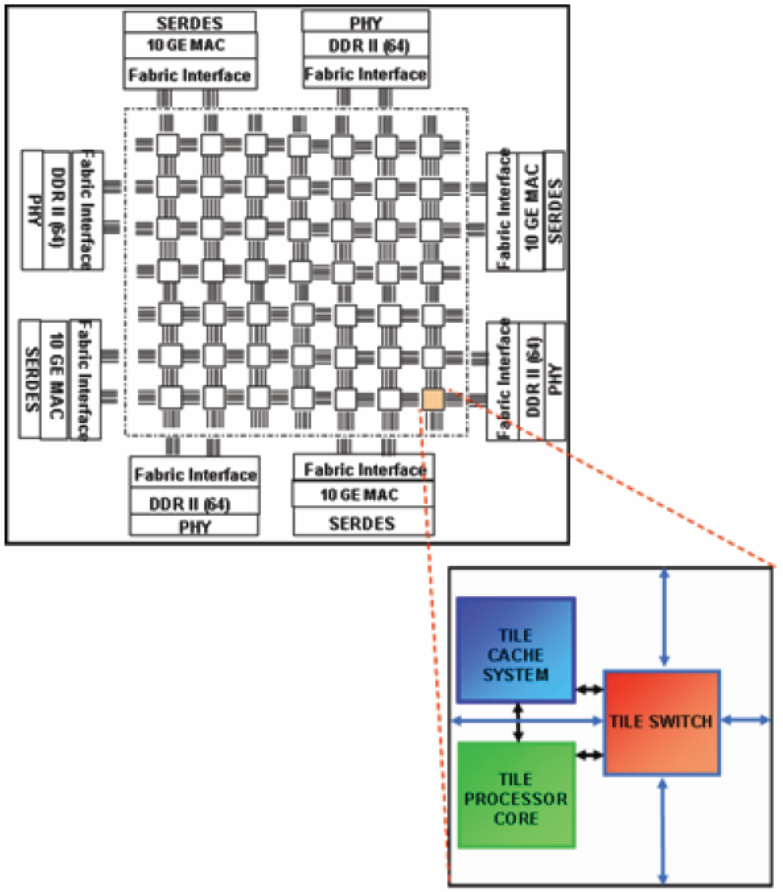
The MAESTRO Chip

- **RHBD version of the Tilera TLR26480 processor**
  - 7 x 7 tile array
  - IBM 9SF 90 nm CMOS process
  - 480 MHz, 70 GOPs, 14 GFLOPs average
  - < 28 Watts Peak (selectable)
    - Possible to no-op cores and reduce power
    - ~ 270 mW per core
  - Integrated floating point unit in each tile processor
    - IEEE 754 compliant, single and double precision
    - Aurora FPU IP
  - 500 Krad TID
  - Demonstrate NASA TRL-6 by December 2010
  - Software compatible with the Tilera TLR26480
    - Reduced number of cores, slower clock speed, added FPU
  - Tilera TLR26480 information can be found at www.tilera.com



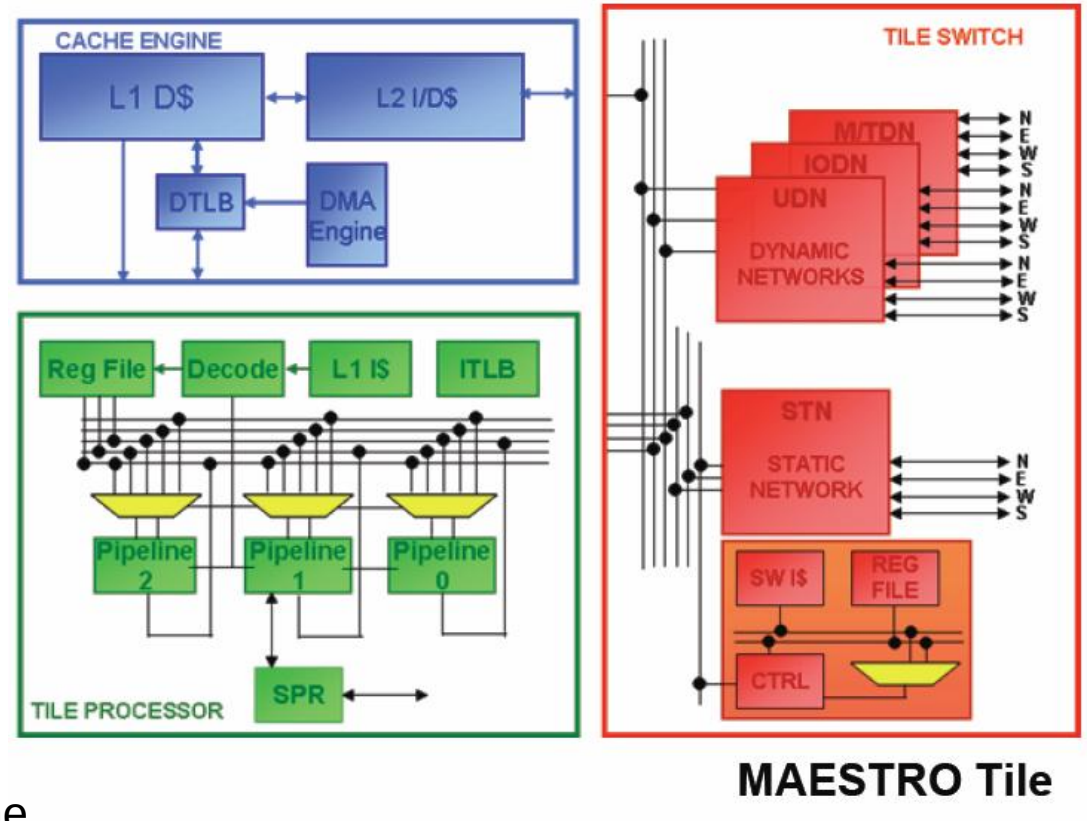
MAESTRO Features

- **Tiled Architecture:**
  - 2-d mesh of processors, connected by low-latency high-bandwidth register-mapped networks
  - Intra tile VLIW performance
  - Multi-tile ILP compilation
  - Inter-module communication acceleration at compile time
- **Processors:**
  - Main processor: 3-way VLIW CPU, 64-bit instruction bundles, 32-bit integer operations
  - Static switch processor: 16-bit instructions
- **Memory:**
  - L1 cache: 2 cycle latency
  - L2 cache: 7 cycle latency
  - Caches not automatically coherent across tiles
  - Tiles can access other tiles' L2 cache ("L3")
  - Off-chip main memory, ~88 cycle latency
  - 32-bit virtual address space per tile
- **IO interfaces**
  - Four integrated XUAI MACs
  - Two 10/100/1000 MACs



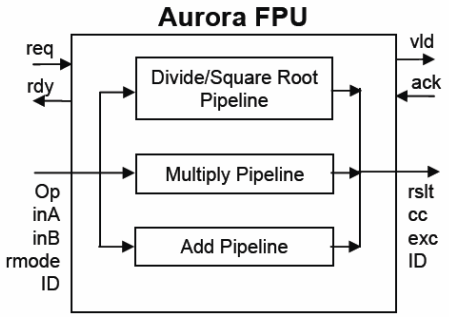
Tile Block Diagram

- **Tile Processor**
  - 3 way VLIW processor
  - 8 KB L1 Instruction cache
  - Instruction Translation Look-aside Buffer (TLB)
- **Cache System**
  - 8 KB L1 Data Cache
  - 64 KB L2 I/D Cache
  - Data TLB
  - DMA Engine
- **Tile Switch**
  - Switch processor
    - 2 KB switch instruction cache
    - Switch TLB
  - Static network (STN)
  - Dynamic networks
    - MDN, TDN, UDN and IODN

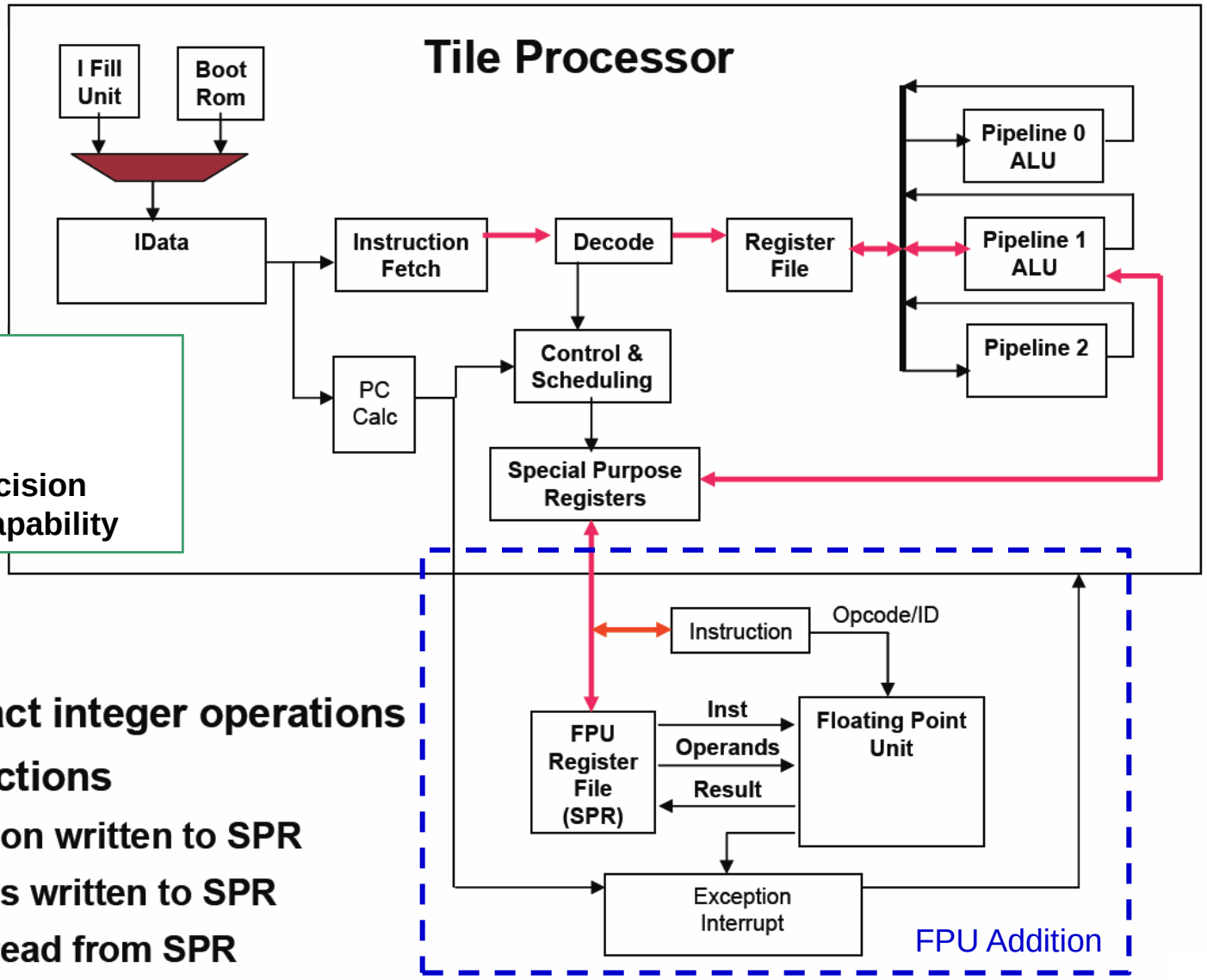


MAESTRO Tile

MAESTRO FPU – Added to Tilera IP



- **Aurora FPU:**
- **Existing Core**
- **IEEE 754 Compliant**
- **Single and Double Precision**
- **Multiply-accumulate capability**

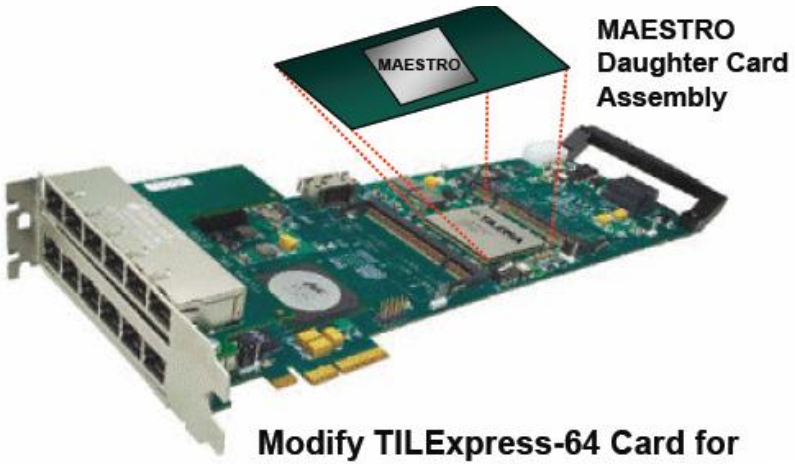


- **Model**
  - **Does not impact integer operations**
  - **No new instructions**
    - **FPU instruction written to SPR**
    - **FPU operands written to SPR**
    - **FPU results read from SPR**

MAESTRO Functional Testing

- **Credence Chip Tester**
  - Test functionality and measure performance
    - Functional operation of MAESTRO
    - Test vectors developed from ModelSim simulations
    - Functional Go / No-Go on vectors for all tests
  - Parametric measurements include:
    - Vol, Voh, Vil, Vih, IoL, Ioh, Iil, Iih
    - Propagation delay
    - Power measurements will be made to validate Physical Compiler power analysis
- **Modified Tilera TILExpress-64 PCIe Board**
  - Greater functional testing than Credence can support
    - High level functional evaluation
    - Software compatibility checking
  - Develop MAESTRO daughter interface card

Boeing Credence Chip Tester



Modify TILExpress-64 Card for higher level functional Test

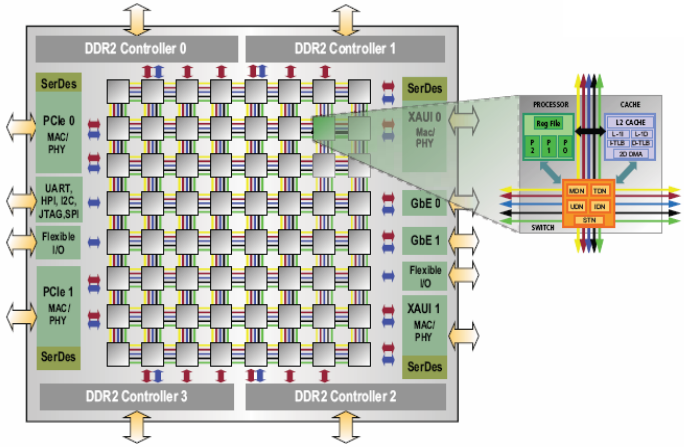
Tilera Products

Information about Tilera products can be found at www.tilera.com

Multicore Development Environment™
Product Brief

TILExpress-64™ Card
Product Brief

TILE64™ Processor
Product Brief



Commercial Development Platform Available from Tilera

OPERA Chip And Development Board Fast Facts

This short brief provides a summary of key hardware and software features present in the initial OPERA development environment (Tilera commercial development board and toolkit). Tilera chip IP has been purchased for US Government space use. Radiation hardening for space use is underway in a project collaborating with DTRA.

OPERA Fast Facts Available from the OPERA Program Office

OPERA Program
Intellectual Property
Rollout Plan

OPERA Intellectual Property (IP) & Software Rollout Plan

- **Benefits to this approach:**
  - Allows industry to rapidly target US Space customers of all types of missions with tailored multicore solutions
    - Space industry base knows its customers best
  - Leverages existing and competitive space computer board markets
    - Space industry has succeeded in productizing PowerPC 750 and 603
  - Encourage growth of competitive multicore architectures market
  - Create innovation and sources of new US Government space processing solutions
    - Quicken commercial/Government acceptance of multicore architectures
    - Prompt new flight computer board development for Govt Space programs
    - Instigate ***multiple*** multicore chip board solutions for Govt Space use
    - **IP restriction – IP can only be used for US Govt Space programs**

OPERA IP Release & Stipulations

- **Initial IP release – November 2008**
  - RHBD Tile IP design files and documentation
  - RHBD Tile test results (functional and radiation)
  - MPI and VSIPL software release with multicore benchmark results

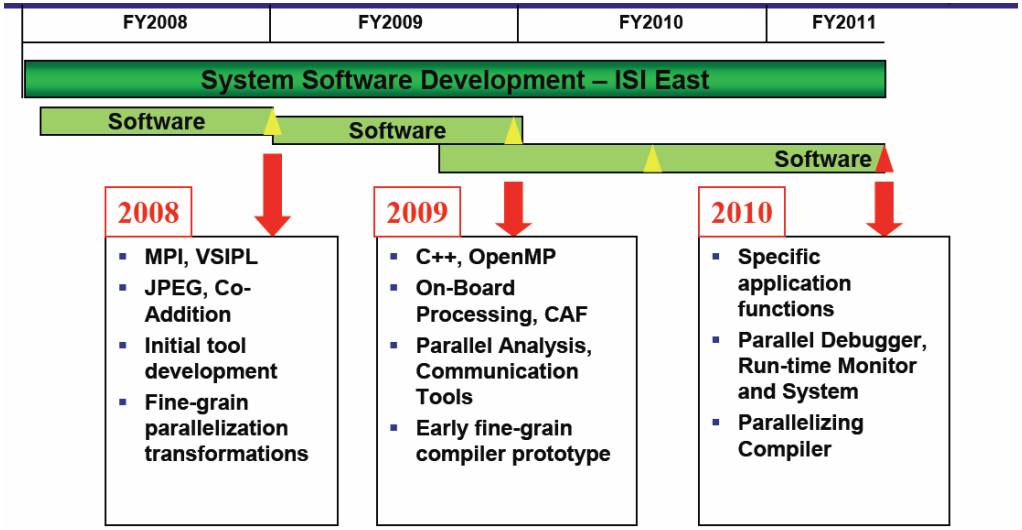
- **In return for the IP release package, contractors are expected to invest their IRAD dollars in this technology area**
  - Contractors who do not authorize IRAD funding
    - Shall return the IP release package by January 31, 2009
  - Contractors who do authorize IRAD funding
    - Will be allowed to keep the IP release package
    - Will be allowed to obtain future IP releases
    - Will be provided a limited number of functioning devices
    - Shall submit their final proprietary 2009 IRAD report to the government by December 31, 2009

OPERA Hardware IP Release Schedule

- **OPERA Tile - Verified IP Release – Nov 08**
  - Single tile design with test wrapper
  - RHBD Program Product Development Vehicle #1 (PDV1)
    - Packaged chip, fully functional tested, IP release will include radiation test results
- **Integrated Test Chip (ITC) - Unverified IP Release – May 09**
  - Design as released for tapeout
- **ITC - Verified IP Release – Nov 09**
  - Packaged chip, fully functional tested
  - IP release will include radiation test results
  - Government to supply limited number of verified devices for test boards
  - Assuming no errors, the ITC chip becomes the MAESTRO device
- **MAESTRO Processor - Unverified IP Release – Apr 10**
  - Design as released for tapeout
  - Includes all OPERA program IP
- **MAESTRO Processor - Verified IP Release – Dec 10**
  - Packaged chip, fully functional tested
  - IP release will include radiation test results
  - Government to supply limited number of verified devices

OPERA Software
IP Release Schedule

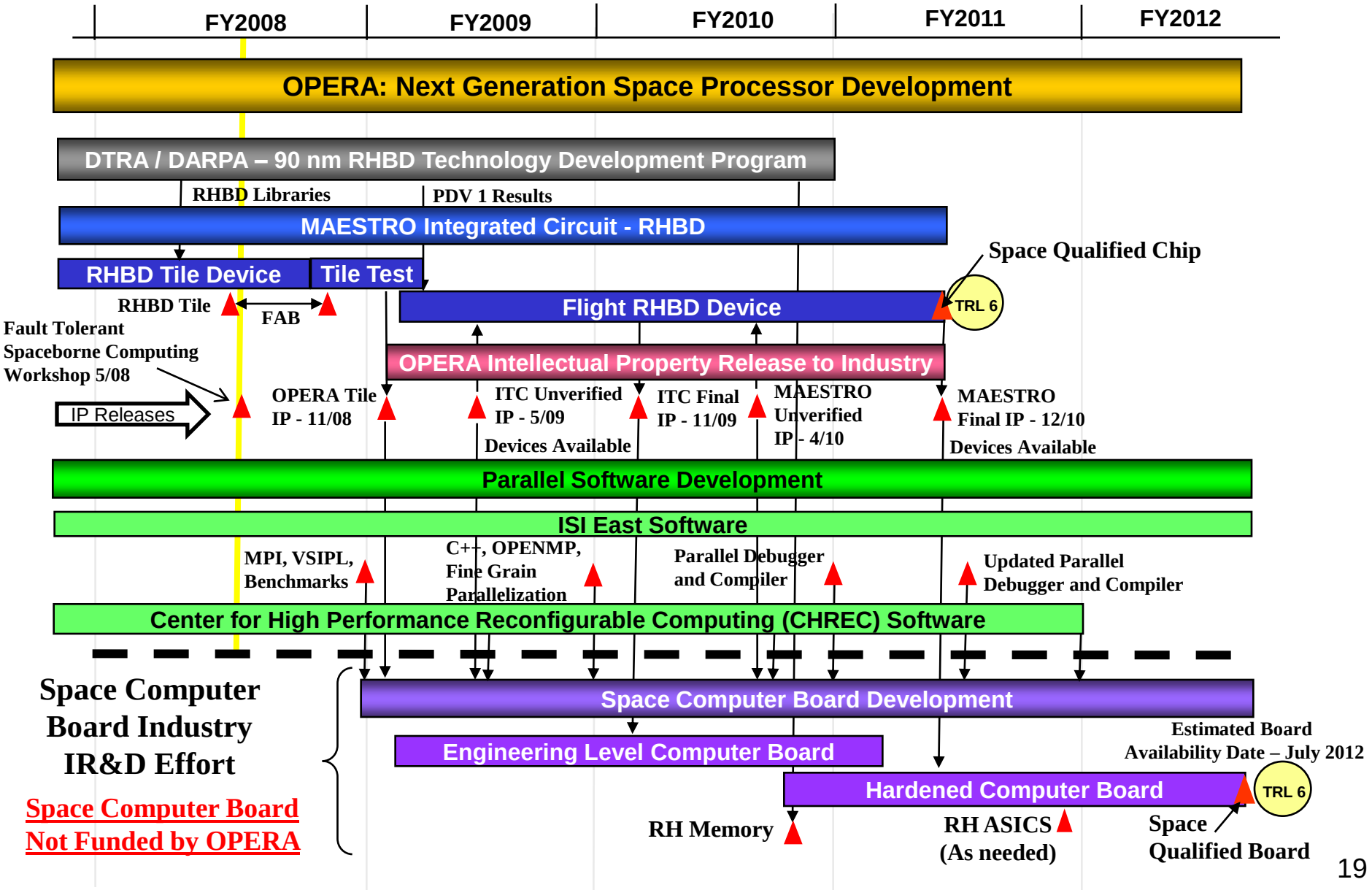
- **Multicore MPI & VSIPL Software & Benchmark Release – Nov 08**
  - Delivery on schedule
- **C++, OPENMP, Fine Grain Parallelization Release – Oct 09**
  - Development effort in progress
- **Parallel Debugger, Compiler Release – Oct 10**
  - Anticipated release date
- **Updated Parallel Debugger and Compiler – Apr 11**
  - Anticipated release date



OPERA Software effort provides a broad range of tools, applications, benchmarks and research activities that significantly advance the state-of-the-art in multi-core software development

More Details Provided in the OPERA Software Presentation

OPERA Program Roadmap



Conclusion

- **MAESTRO is a RHBD version of the Tilera TLR26480**
  - 7x7 array of homogeneous MIPS-like processor cores in a mesh style architecture
    - 480 MHz, 70 GOPS, 14 GFLOPS, ~ 20 Watts average
  - Each tile processor is a capable, RISC, VLIW general purpose processor
  - The architecture is scalable and lends itself well to systolic processing such as processing streaming data from a sensor
  - Processor also well suited to complex data management tasks
  - Longest wire is the system is no greater than the width of a tile
    - Ensures high clock speeds and continued scalability
- **OPERA IP rollout scheduled to start November 2008**
  - Space computer board community interest being gauged
  - Communicate 1 on 1 with interested companies / agencies as needed
  - Government is obtaining preliminary industry commitments for IP
    - July timeframe
  - Interested companies should contact OPERA program office
    - **For OPERA questions, do not contact Tilera, contact the Gov't PM**

Government OPERA Contact

Dagim Seyoum
OPERA Program Manager
US Government
OPERA_Rocks@Mac.com
1-800-306-6990 ext. 6072

Questions ??