Abstract for proposed plenary talk at 5th Workshop on Fault-Tolerant Spaceborne Computing

Innovations in Advanced Spaceborne Computing

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Faced with an expanding and increasingly challenging list of mission requirements in sensor processing and autonomous processing, be it earth science, space science, or defense missions, the need for on-board, high-performance computing in space has grown rapidly in recent years. Of course, unlike terrestrial systems, the harsh environment and extremely limited resources on a space platform make the design, deployment, and operation of such systems uniquely challenging.

Researchers in the NSF Center for High-Performance Reconfigurable Computing (CHREC) at the University of Florida, in partnership with their corporate and government partners in the space industry, are investigating, developing, and evaluating a variety of innovative technologies to help address these challenges in terms of new concepts, methods, devices, systems, and tools. Two of the major themes in this research program are: (1) adaptive systems, recognizing that the dynamic nature of the space environment suggests solutions that can dynamically adapt to improve performance, dependability, and energy-efficiency as mission and orbital conditions change; and (2) use of commercial off-the-shelf (COTS) technologies.

This presentation will introduce and provide highlights from on-going research projects and new technologies in the space research groups of CHREC at Florida, with primary focus upon processing devices, metrics, and benchmarks for space-based processing. Topics to be highlighted will include:

- Metrics, benchmarking, and tradeoffs in fixed- and reconfigurable-logic devices for space
- Theory and framework for Pareto optimization of performance, power, and dependability in the design of space-based processing systems and applications
- Adaptive and durable communications and management middleware for heterogeneous and distributed space-based processing, from small satellites to clusters or constellations
- Structures for reconfigurable fault tolerance to dynamically maximize system performability
- Low-overhead, algorithm-based fault tolerance in reconfigurable hardware
- Hybrid COTS-based processing architecture for small satellites; space-based applications
- Spatial and temporal fault injection for testing of reconfigurable-logic devices
- New initiatives such as asynchronous circuits and field-programmable gate arrays with dual-modular redundancy