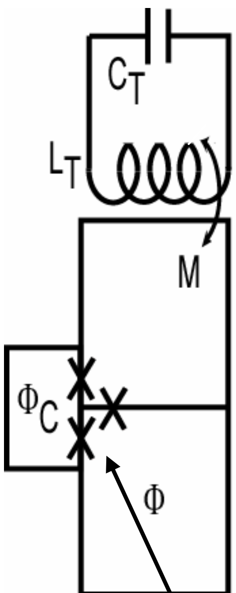
Prospects for Computing Beyond CMOS

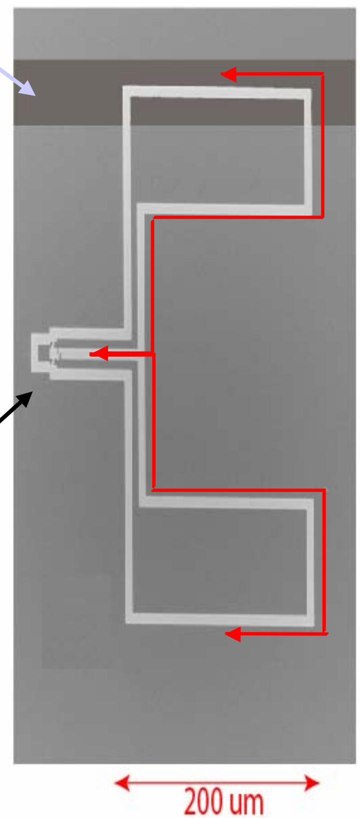
Thomas N. Theis,
Director, Physical Sciences, IBM Research

An exploratory quantum device

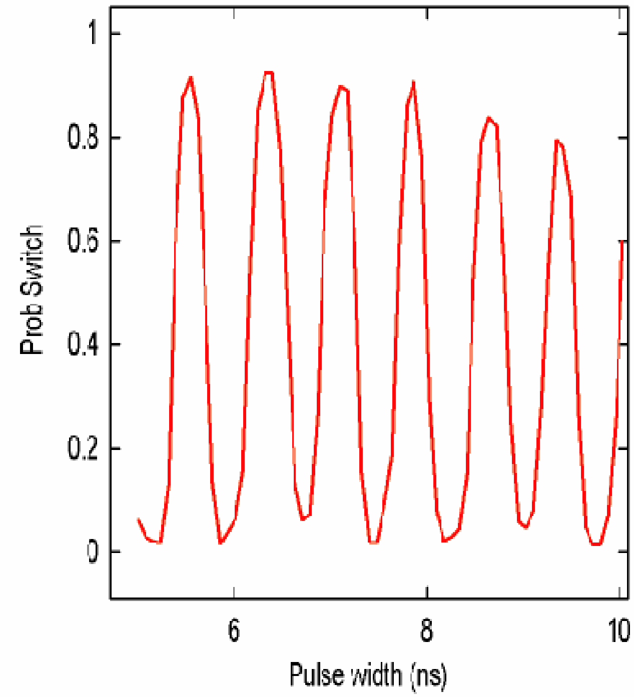
IBM Josephson Junction Qubit

Transmission line stabilizer





Three 100 nm
Josephson junctions

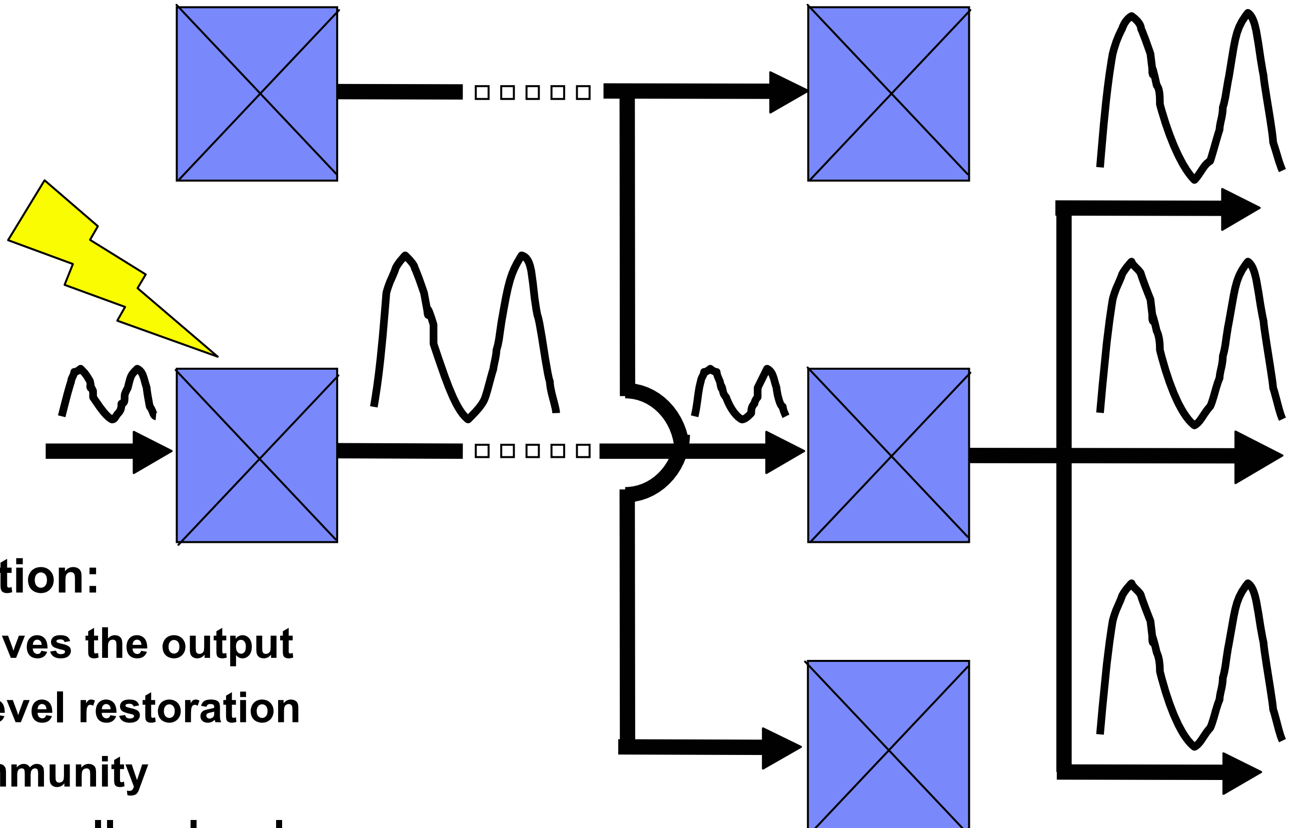


Measured probability of finding the system in the “current flowing out” state

5 criteria for building a practical quantum computer
(The DiVincenzo Criteria)

1. Well-defined extendible qubit array (stable memory)
2. Preparable in the "000…" state
3. Long decoherence time (>10^4 operations)
4. Universal set of gate operations
   ➔ extremely precise control of dynamical phase
5. Single-quantum measurements (read out)

The criteria for historically successful classical logic devices are very different.



Amplification:

- ⇨ **Input drives the output**
- ⇨ **Signal level restoration**
- ⇨ **Noise immunity**
- ⇨ **Global as well as local communications**

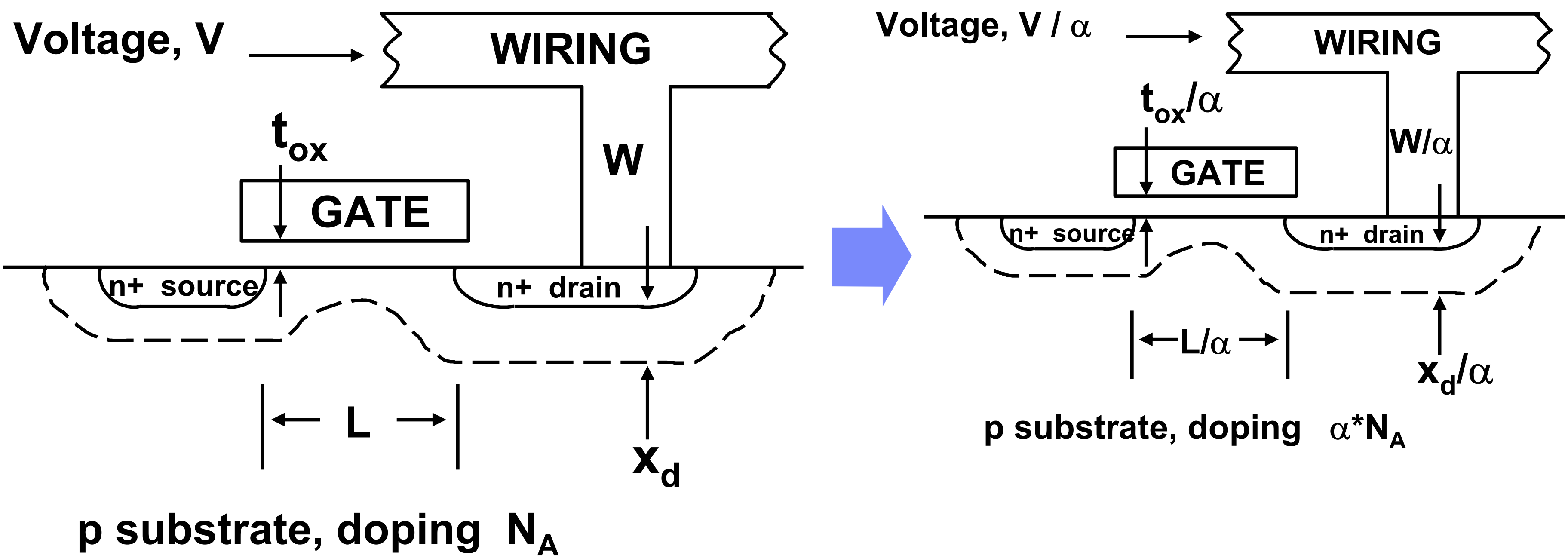
After H.-S. P. Wong, "Novel Device Options" in Sub-100nm CMOS Short Course, *IEDM*, 1999

Topics

- The extension of silicon CMOS technology
- The search for the "ultimate" FET
- Prospects for adiabatic switching and reversible logic
- "Beyond the FET":
  The Nanoelectronics Research Initiative and the search for better devices for reversible logic

Transistor Scaling

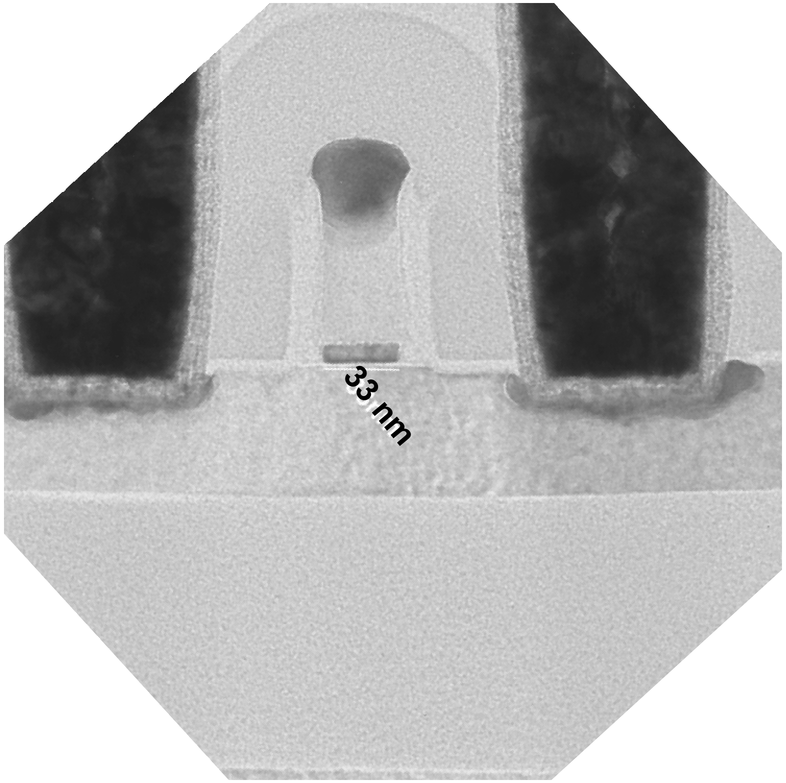
Dennard, et al., 1974



RESULTS:

Higher Density:	α^2
Higher Speed:	α
Lower Power: per circuit	$1/\alpha^2$
Power Density:	**Constant**

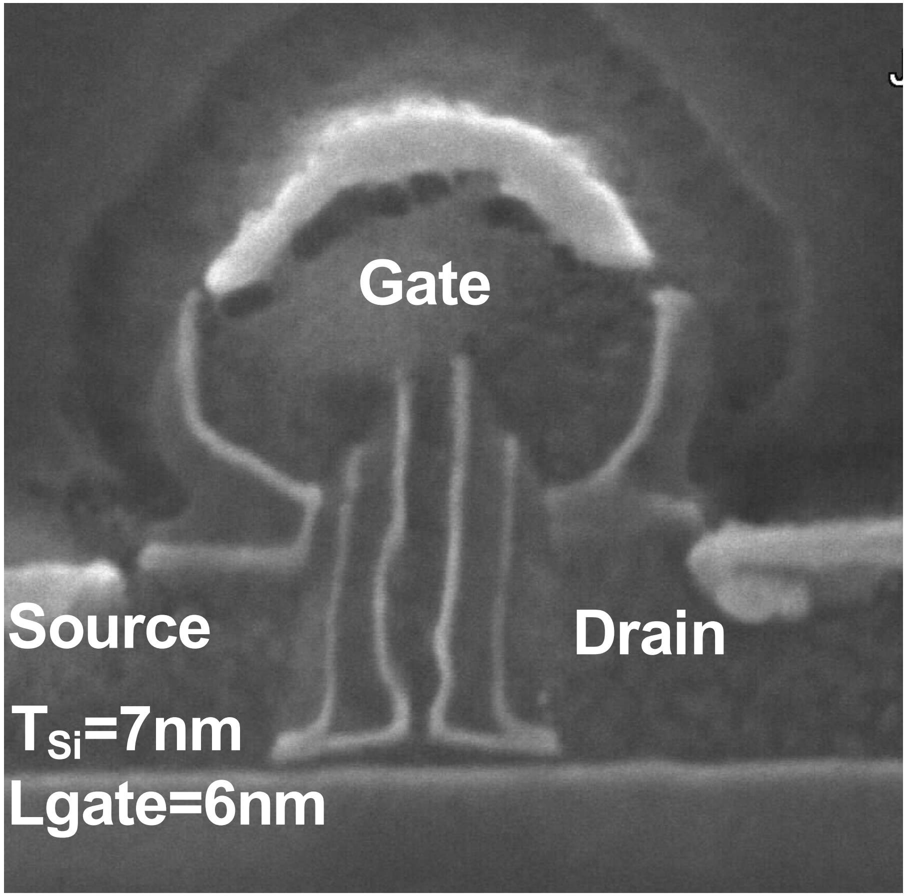
The silicon transistor in product development …



45 nm technology generation

Chudzik et al., VLSI 2006

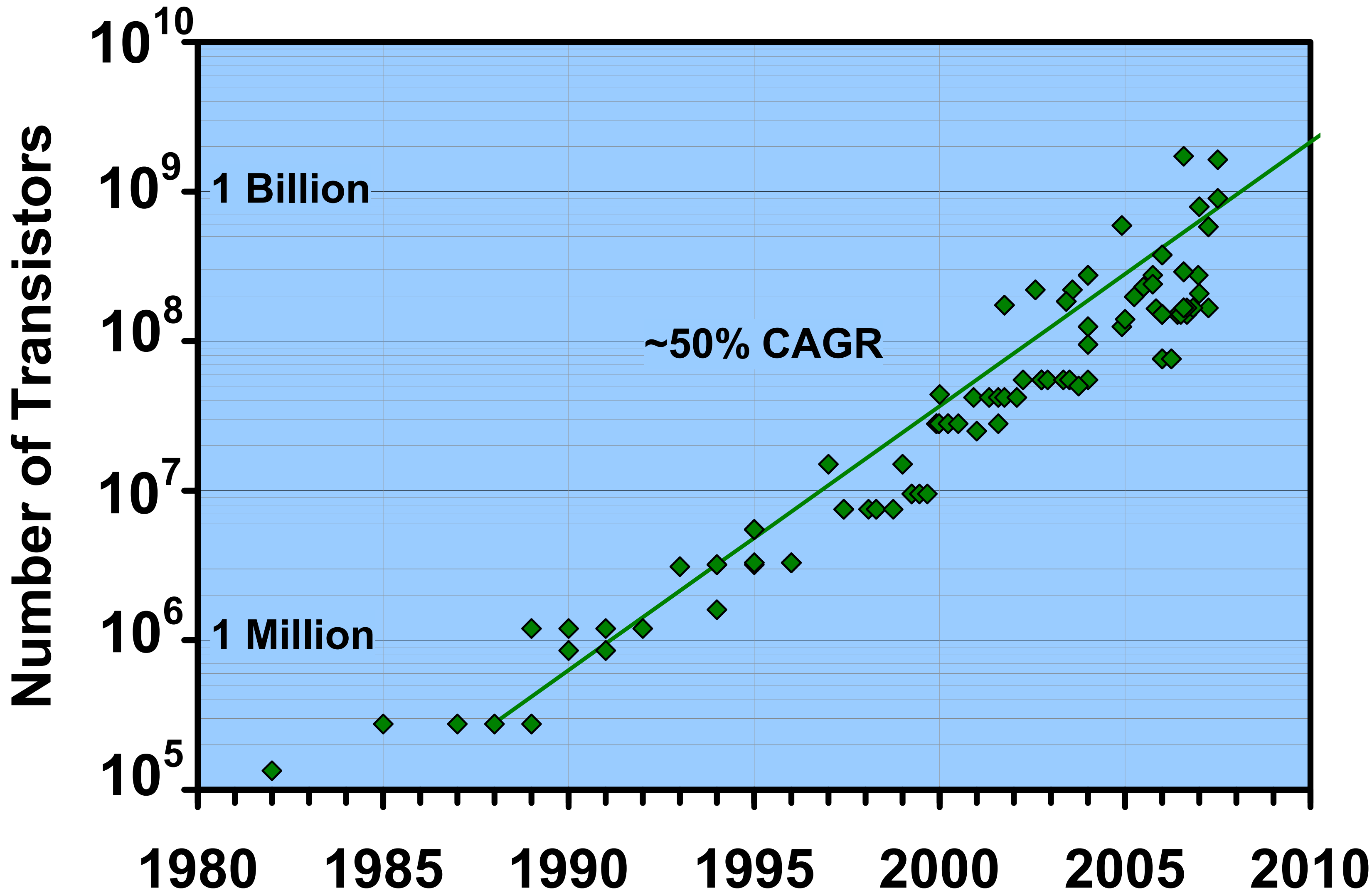
… and in the lab.



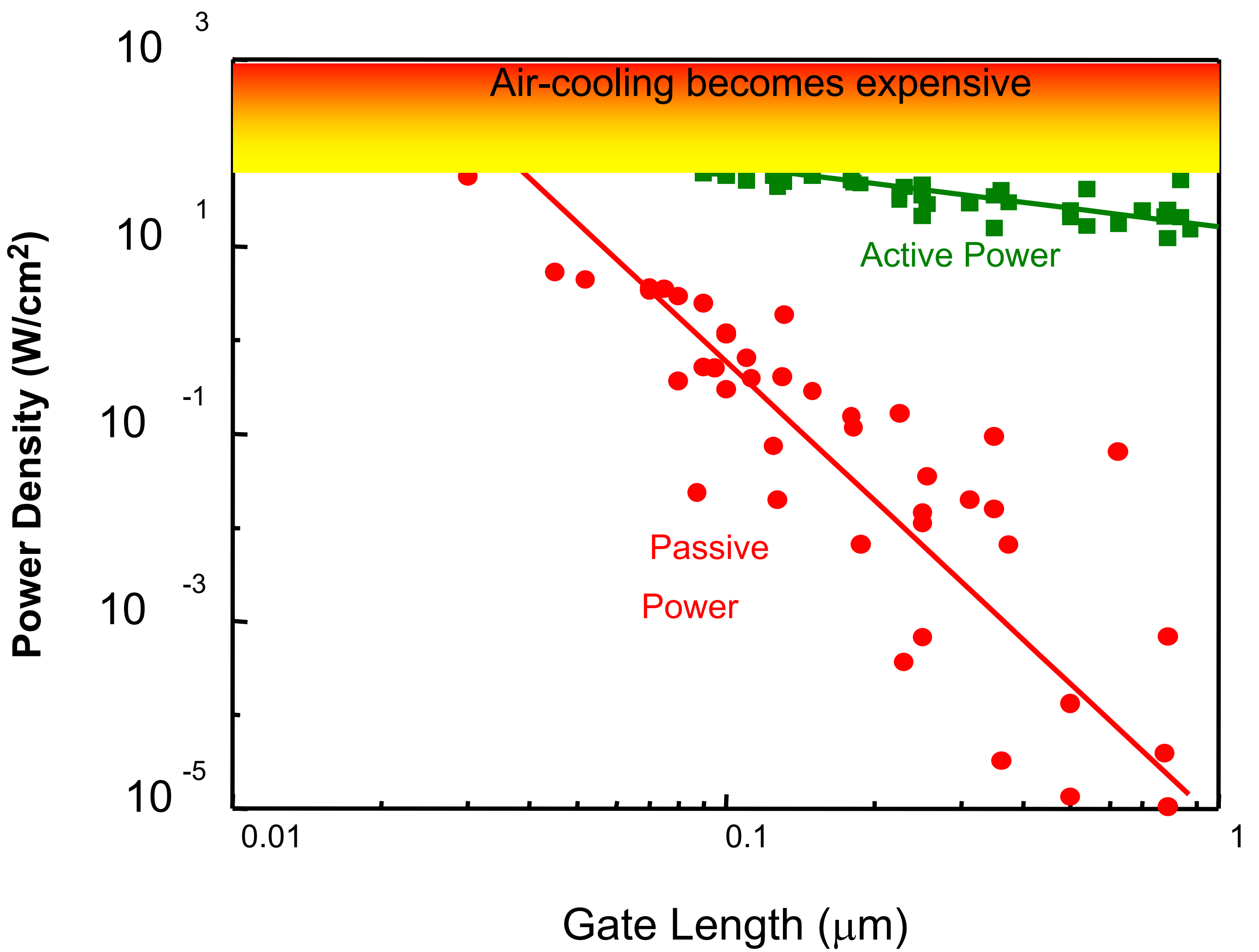
B. Doris et al., *IEDM* , 2002

Microprocessor Transistor Count

Lithography continues to deliver density scaling.

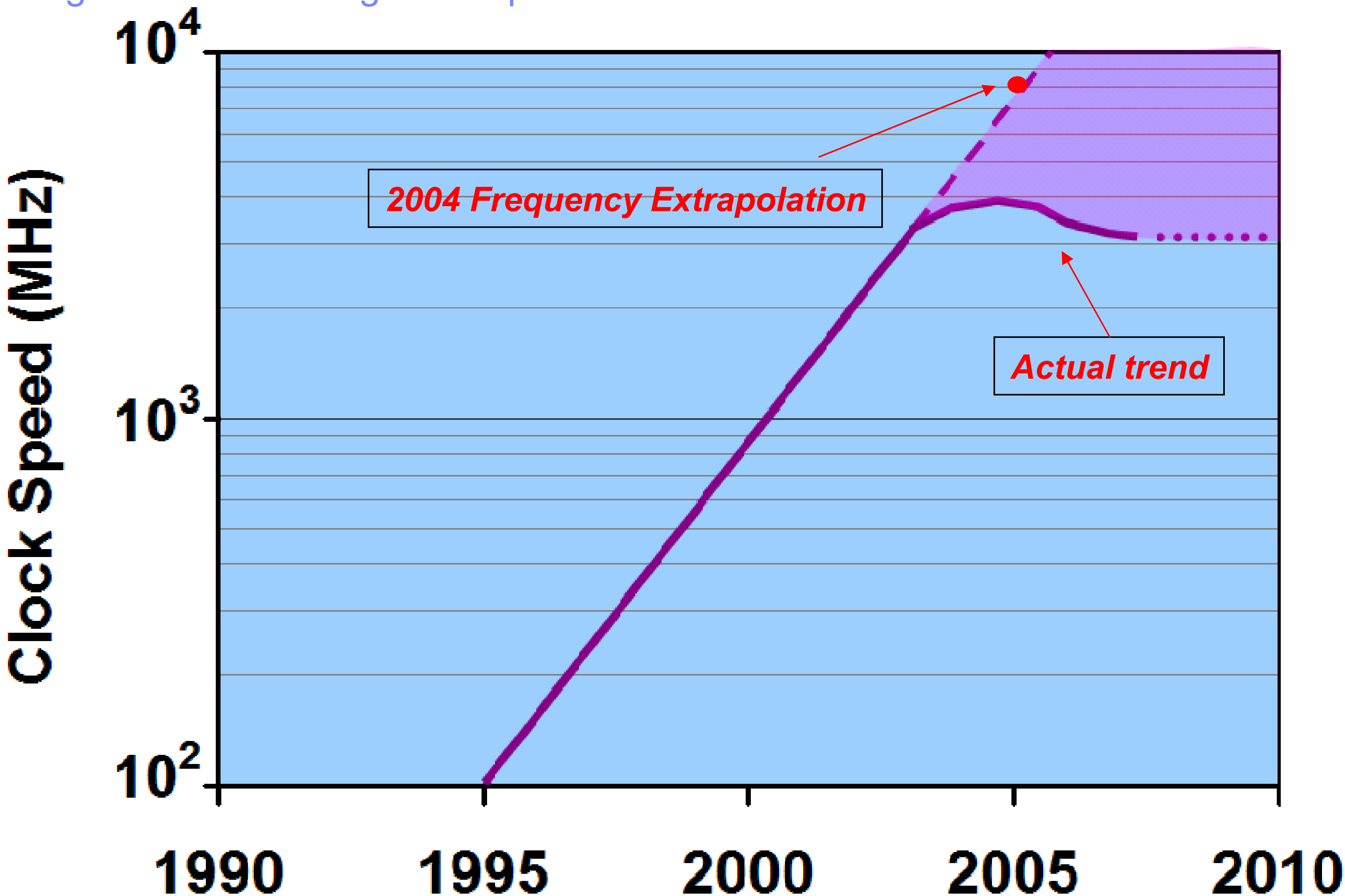


Still, we are approaching some limits.

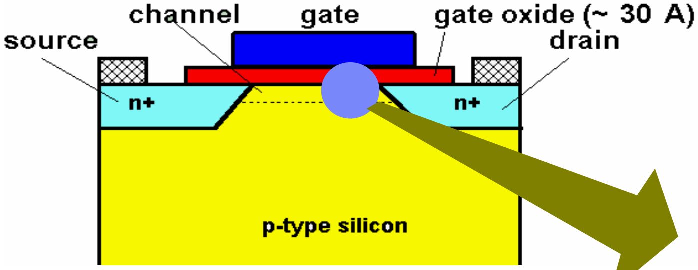


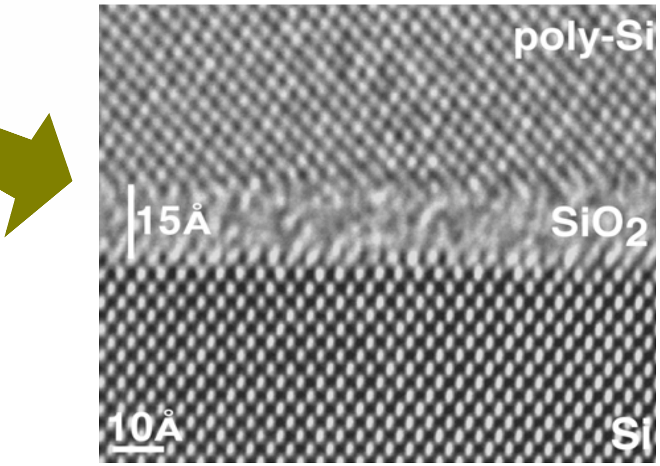
Microprocessor Clock Speeds

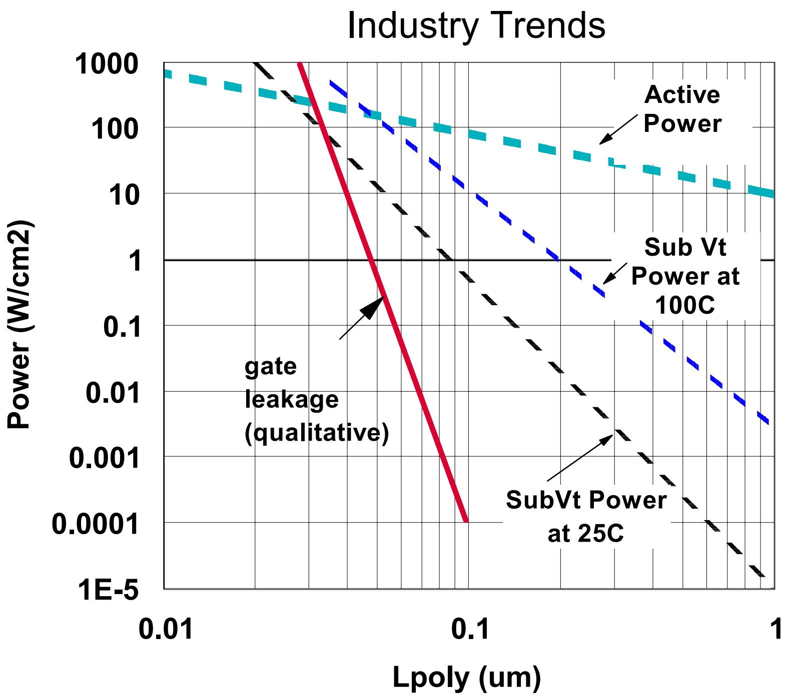
Cooling costs are limiting clock speeds



The Problem with Passive Power Dissipation: The Inability to Scale Atoms

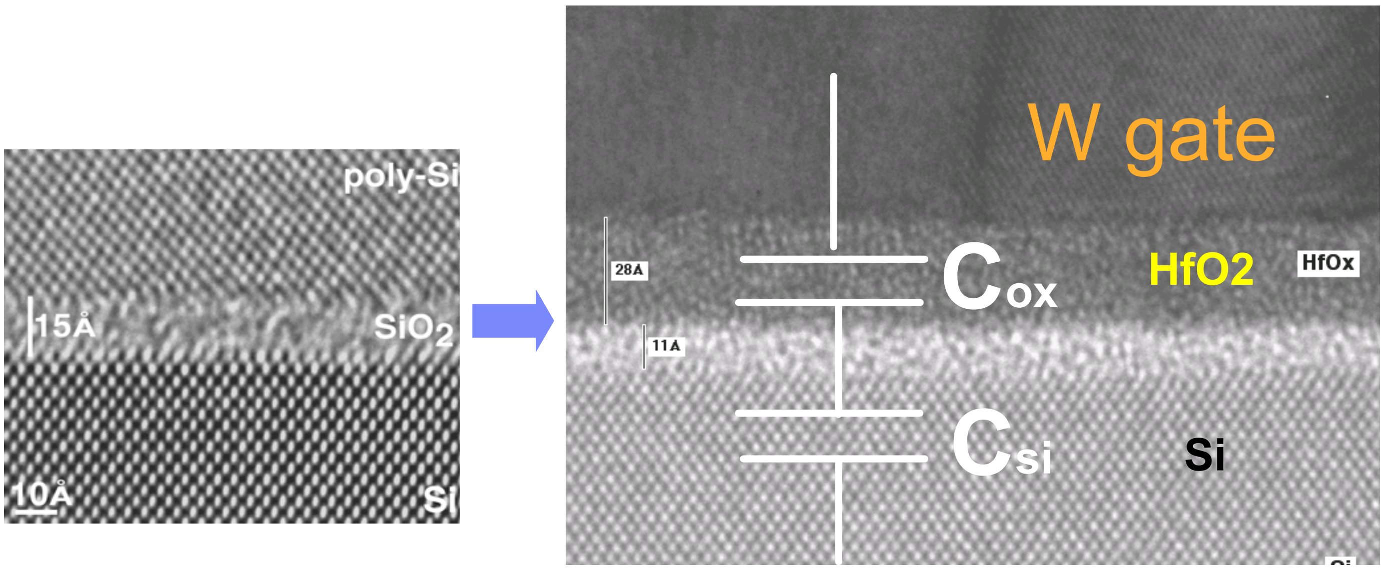






- Direct tunneling through the gate insulator will dominate static power dissipation.
- Single atom defects cause local leakage currents 10 – 100x higher than the average current, impacting reliability and increasing variation between devices.

The Work-Around:
High-k Insulator / Metal Gate Stack

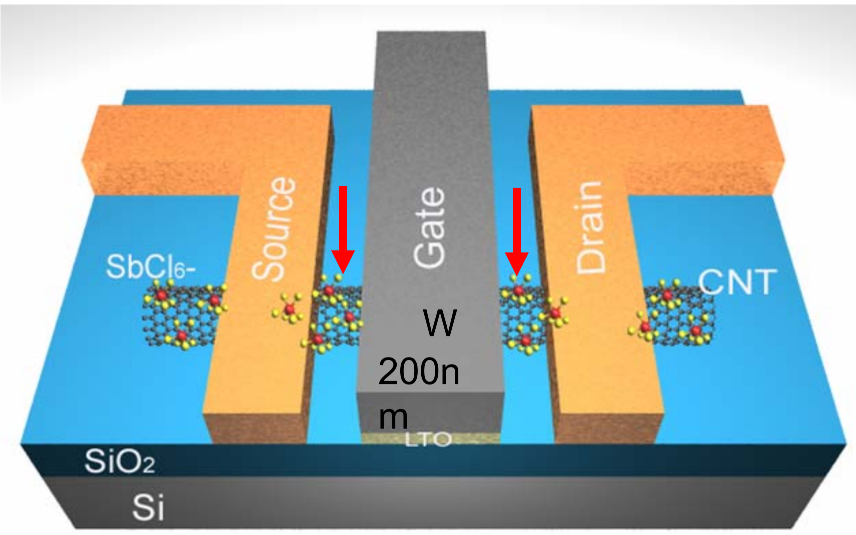


$$C_{gate} = \varepsilon A/d$$

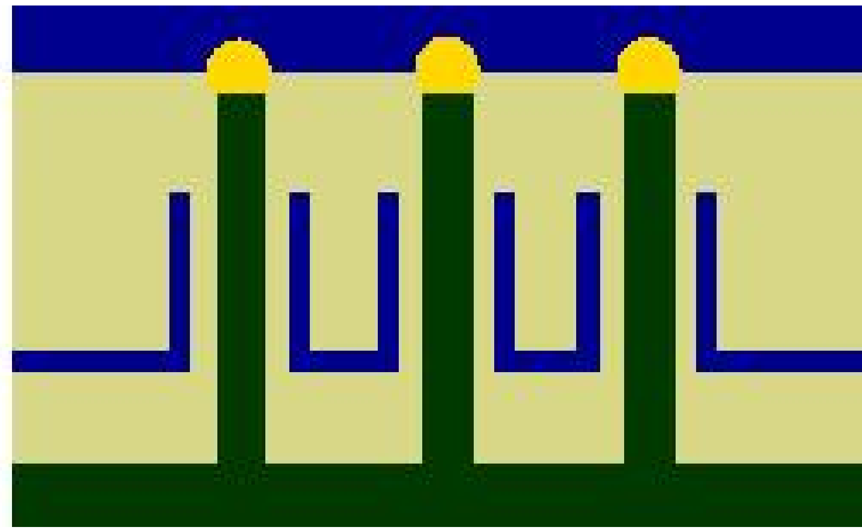
Decrease leakage currents.

Reduce short channel effects.

The Quest for the Ultimate FET



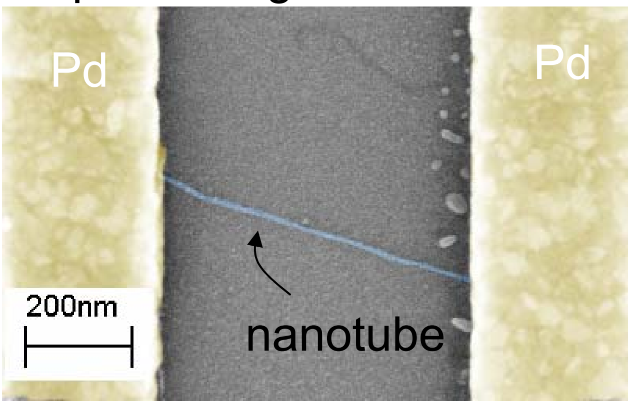
Self-Aligned Carbon Nanotube FET:
Extension Contacts Based on
Charge-Transfer Chemical Doping



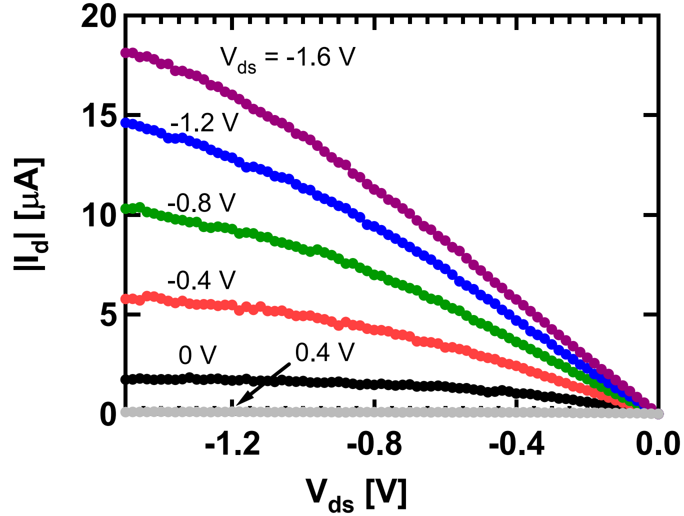
Vertical Transistor
Based on Semiconductor Nanowires

Intrinsic Performance of Carbon Nanotube FETs

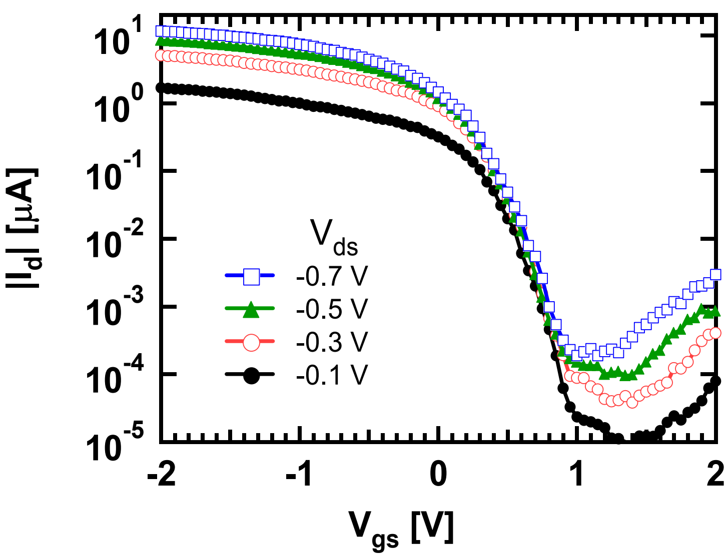
Simple back-gated CNTFET



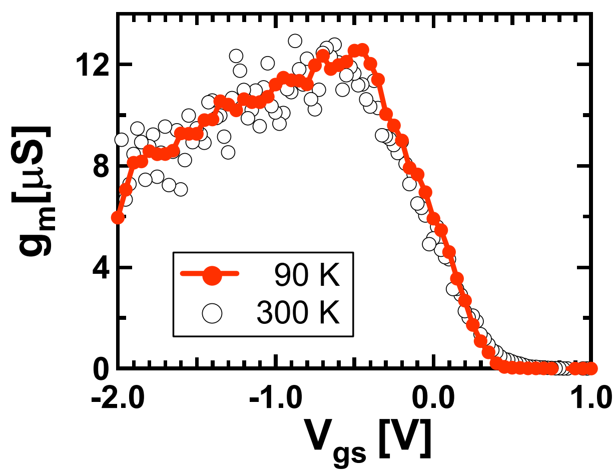
Output Characteristics



Subthreshold Characteristics



Temperature dependence



Yu-Ming Lin *et al.* (IBM), EDL 2005

Intrinsic Switching Speed of CNFETs

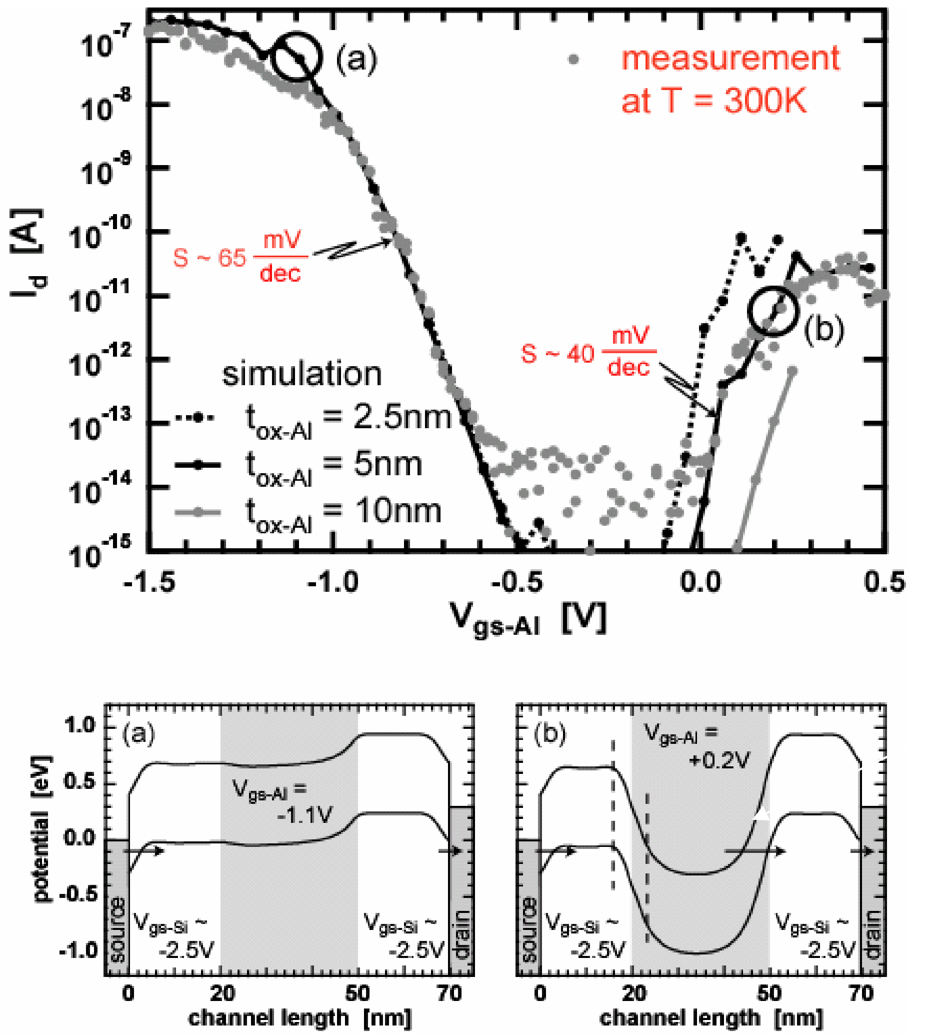
Cut-off Frequency $f_T = \dfrac{g_m}{2\pi C_g}$ C_g : gate capacitance

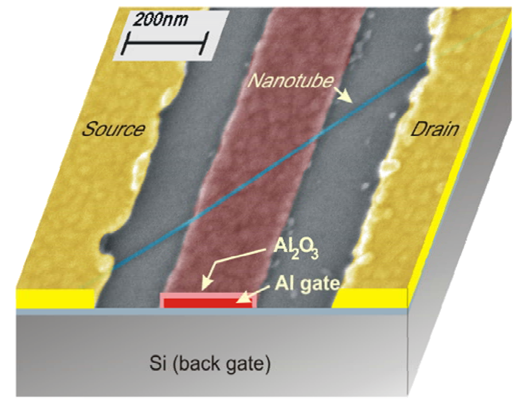
	Lin et al. (IBM)	Javey et al. (Stanford)	Seidel et al. (Infineon)
Diameter	~ 1.8 nm	~ 1.7 nm	~ 1.1 nm
Gate Dielectric	10-nm SiO_2	8-nm HfO_2	12-nm SiO_2
Maximum g_m	12.5 μS	27 μS	3.5 μS
C_g/L	38 pF/m	120 pF/m	32 pF/m
f_T @ L_g = 65 nm	**800 GHz**	550 GHz	260 GHz

Yu-Ming Lin *et al.* (IBM), EDL 2005

Carbon Nanotube FET:

Potential for greatly improved turn-on characteristics (low-voltage operation)





Dual-Gate
CNTFET

J. Appenzeller, Y.-M. Lin,
J. Knoch, and Ph. Avouris,
Phys. Rev. Lett. **93**, 196805 (2004)

Subthreshold Slope

$$S = dV_g / d(\log_{10} I)$$

$$= (dV_g / d\psi_s)\ (d\psi_s / d(\log_{10} I))$$

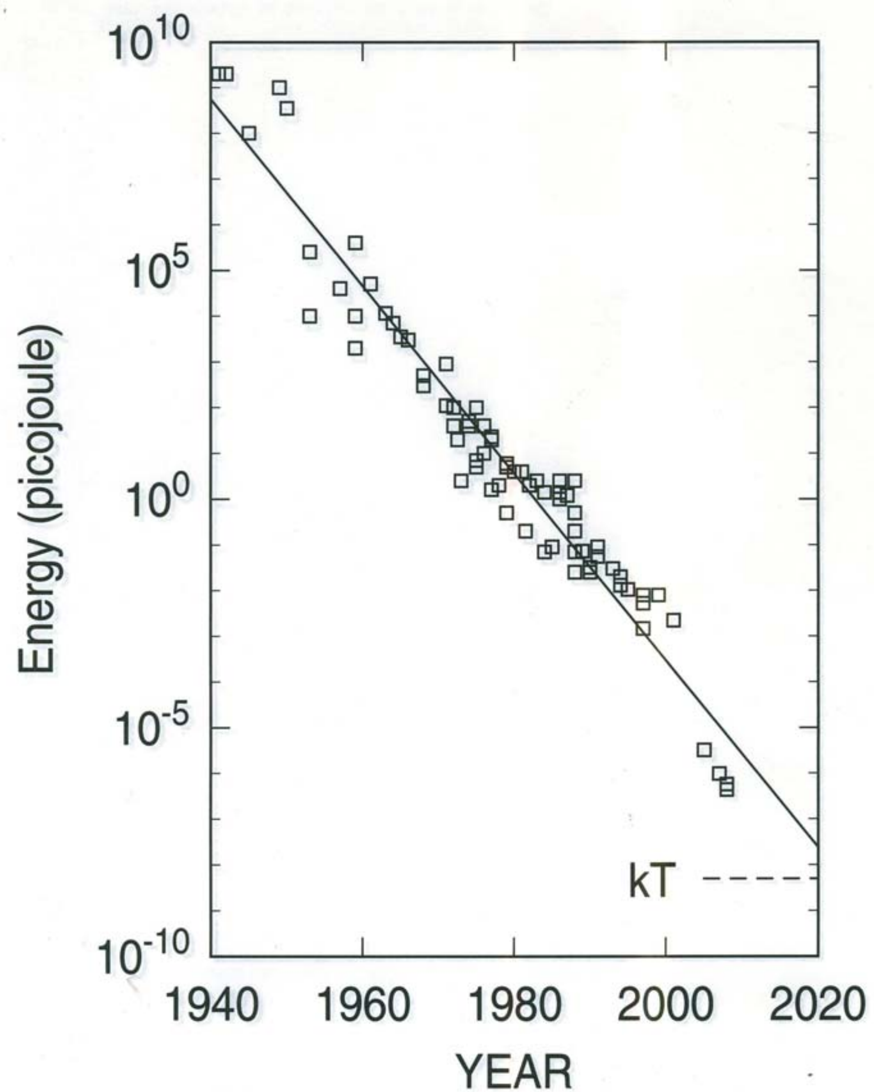
"body factor" m

surface potential
in the channel

$$d\psi_s / d(\log_{10} I) = 60 \text{ mV/decade}$$

at room temp.

FETs approach the "kT" limit



Data compiled by R. Keyes, IBM Research

Can we operate FETs near or below the kT “limit”?

Two paths

1. Conventional Logic:

   Reduce the stored energy, ½ CV^2, toward the kT limit, accept the reduction in switching speed, and use redundancy and error correction to keep the error rate in bounds. (Refrigeration is allowed, but this makes economic sense only if *total* power dissipation is reduced.)

2. Reversible Logic:

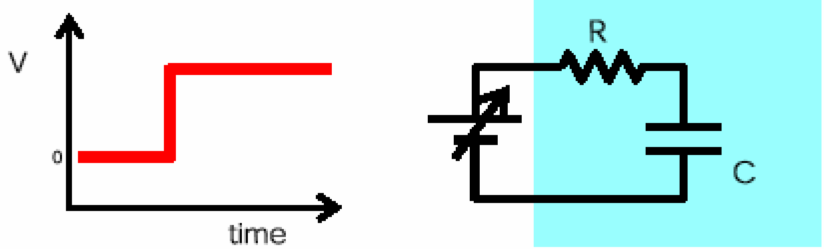
   Maintain ½ CV^2 well above kT, implement adiabatic switching, energy-conserving reversible logic circuits, and energy-recovering (i.e. resonant circuit) power supply to reduce energy losses per switching event to ~ kT or *below*.*

* Note: Dissipation > kT per logical operation is *not* a thermodynamic limit.
It is a practical limit for computing architectures that are not logically reversible.

Adiabatic Charging

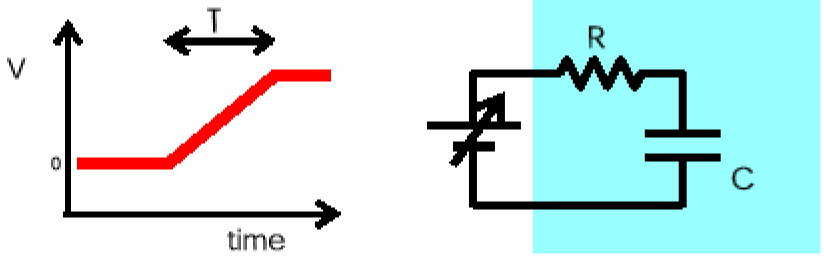
How much energy must be dissipated to charge a capacitor?

Abrupt method



$$E = \frac{1}{2} C V^2$$

Quasi-static Charging



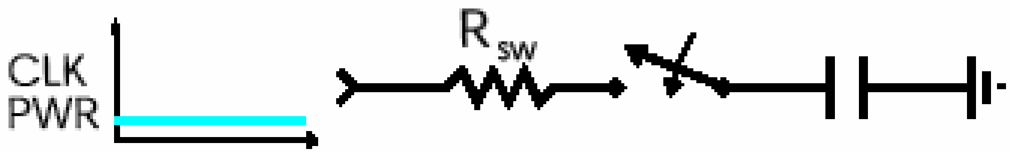
$$E = \frac{1}{2} C V^2 \left(\frac{2RC}{T}\right)$$

(T >> RC)

Adiabatic Switching

To take advantage of quasi-static charging in logic, there are 2 steps:

First, close switch ($V_{CLK} = V_{CAP}$)



Then, apply clock power (slowly)

Rule 1: never close a switch (turn on an FET) while there is voltage across it.

Rule 2: don't ramp the voltage too quickly.

David Frank, IBM Research

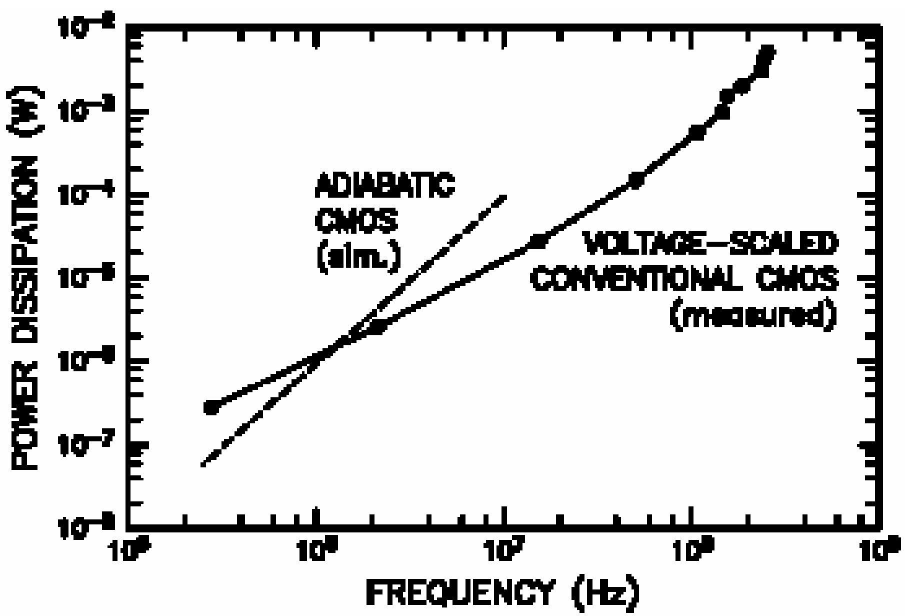
Applications of Adiabatic Charging

- Drive specific capacitances which cause large dissipation.
  - Power supplies
  - Energy conserving data bus drivers

- Broadly implement reversible logic.
  - Retractile cascade, reversible pipelines (easy)
  - High-efficiency regenerative power supply (difficult)

Reversible Logic: Implementation with FETs

- It is conceptually possible to build general purpose reversible computers with energy dissipation per operation going asymptotically to zero as frequency goes to zero.
- But, frequency must be reduced by about 1/1000 to achieve benefits with respect to conventional approaches to CMOS logic.

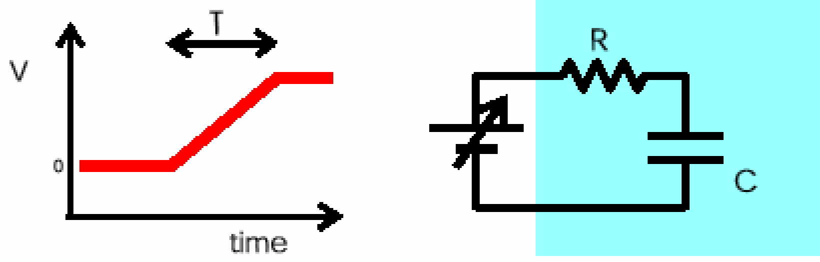


Dissipation of 4 bit ripple counter (D. J. Frank, 1995)

Adiabatic Computing

Energy dissipation depends on the physics of the device!

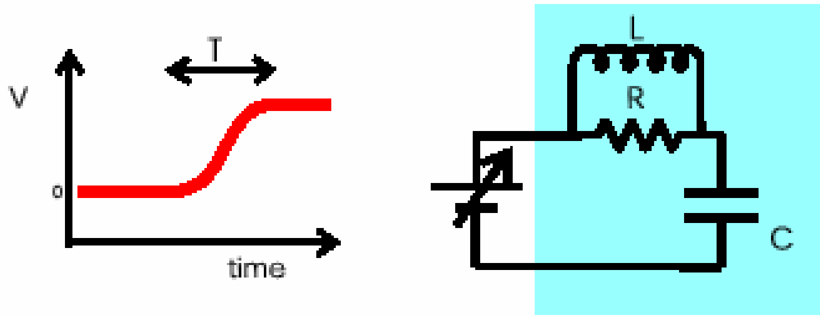
Quasi-static Charging



$$E = \frac{1}{2} CV^2 \left(\frac{2RC}{T}\right)$$

This assumes T >> RC.

Quasi-static Charging + Superconductivity



Charging through a super-conductor, which behaves as an inductor and resistor in parallel.

$$E = \frac{\pi^4}{8} CV^2 \frac{RC(L/R)^2}{T^3}$$

This assumes T >> RC and T >> L/R.

Energy-time trade-off depends strongly on device physics!

DJ Frank, MIT Workshop on Reversible Computation, February 14, 2005

Will there be a successor to the FET?

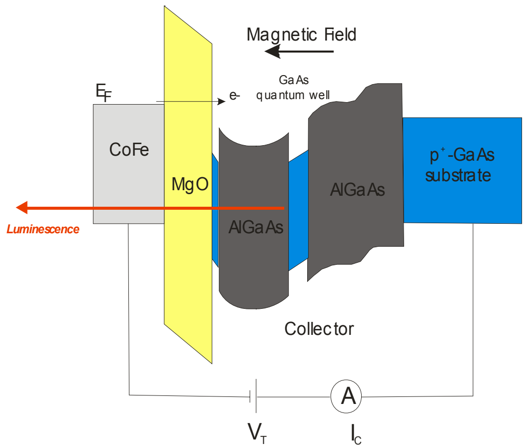
- Many have written about this subject.

- An article by George Bourianoff ("The Future of Nanocomputing", IEEE Computer 36, pp. 44–53) sparked discussions within the SRC regarding the objectives of a new research program – the Nanoelectronics Research Initiative (NRI) – which would stimulate the exploration of devices "beyond the FET".

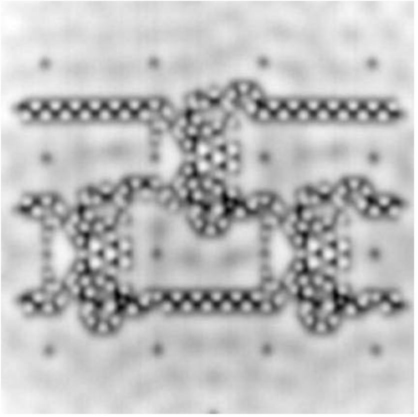
→ computational state vectors other than electronic charge

Beyond Charged-Based Logic?

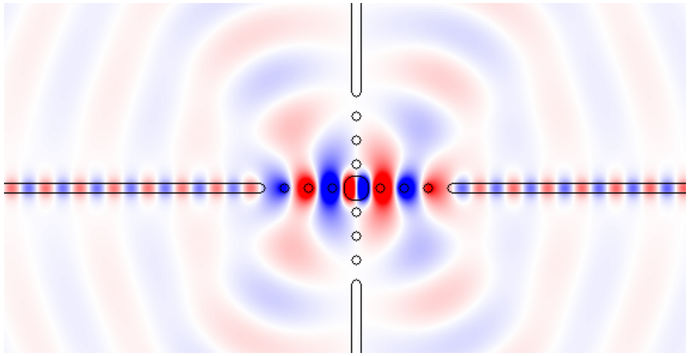
- Spintronics



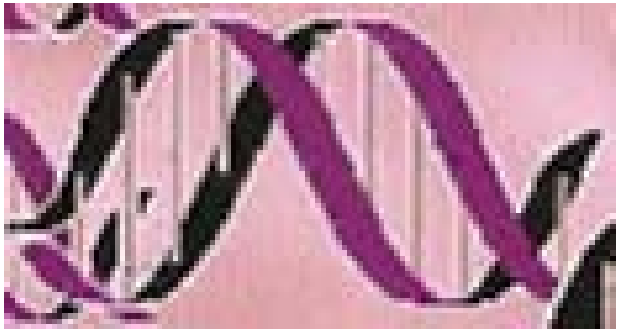
- Nanomechanics



- Plasmonics



- DNA Chemistry



Nanoelectronics Research Initiative (NRI)

- AMD, Freescale, Micron, TI, IBM, Intel
  → Joint Industry funding of University Research

- Promoting both
  - Invention / Discovery (distributed research, “let many flowers bloom”)
  - Proof of Concept (focused university consortia with outstanding facilities)

- “Extend the historical cost/function reduction, along with increased performance and density … orders of magnitude beyond the limits of CMOS”
  - Computational State Vectors other than Electronic Charge
  - Non-equilibrium Systems
  - Novel Energy Transfer Mechanisms
  - Nanoscale Thermal Management
  - Directed Self-assembly of such structures

A device that switches much faster than the ultimate transistor must dissipate much less power per switching event than the ultimate transistor.

- Fast, near-adiabatic switching
- Energy-conserving (reversible) logic
- Precise control of dynamical phase over many logical operations
- Fine-grained error correction

A device that can be integrated much more densely that the ultimate transistor will be much smaller than the ultimate transistor.

- “Classical” logical states approximated by small ensembles of quantum states
- Quantum decoherence contributes to error rate
- Fine-grained error correction

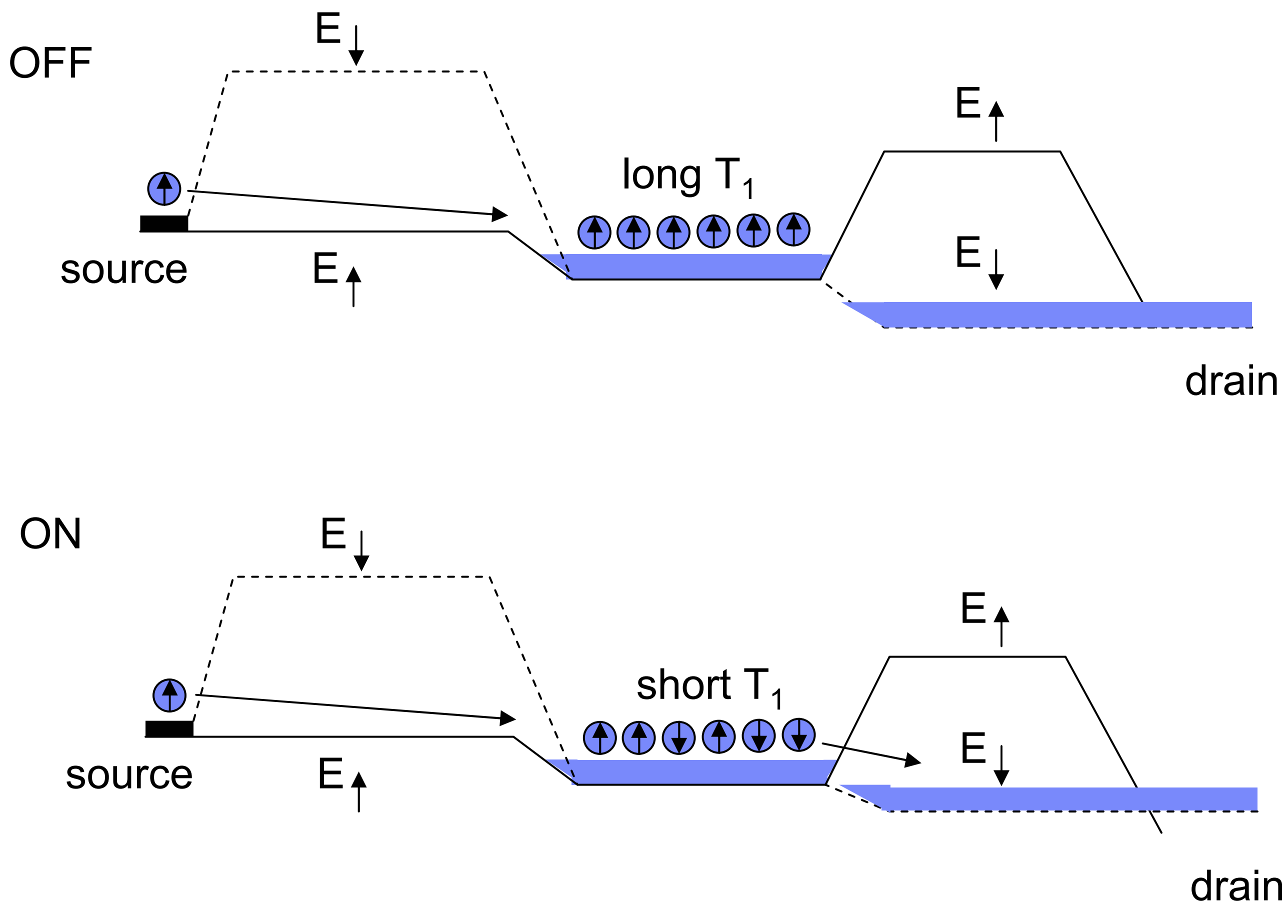
The is much excitement regarding the possibility of spin-based logic devices.

- "If the operations are done coherently the minimum switching energy derived for charge-based information processing does not apply."
- "…the switching energy of a fast spin-based device can be much closer to the fundamental limit than a charge-based device"

D. D. Awschalom and M. E. Flatte,
Nature Physics 3 (153 – 159) March 2007

Spin-based insulated gate field effect transistor

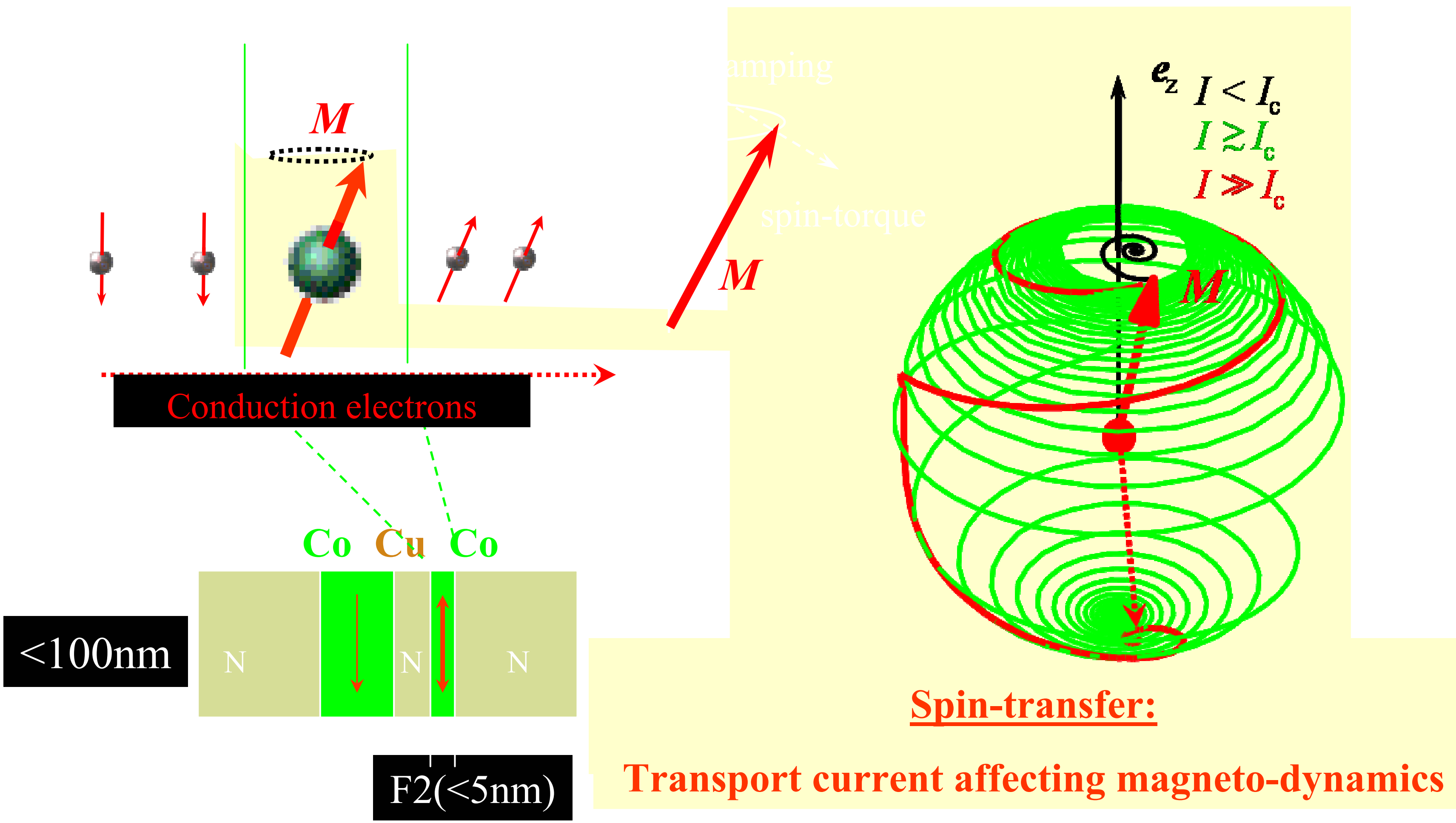
K.C. Hall and M.R. Flatte, APL 88, 162503 (2006)



Spin angular momentum transfer and spin-torque:

J. C. Slonczewski, J. Magn. Magn. Mater. **159,** L1 (1996); ibid, **195**, L261 (1999).

J. Z. Sun, J. Magn. Magn. Mater. **202**, 157 (1999); Phys. Rev. B62, 570 (2000) , Nature **425**, 359 (2003).



Unknowns

- The device
  (So far, nothing smaller or faster than an FET can reliably gate another device.)
- The non-local interconnections
- Energy cost of the control system.
  – Analogous to a clock in a conventional circuit? … or are there reversible versions of non-clocking (handshaking) circuits?
  – Stringent timing requirements and limits on energy dissipation?
- Energy cost of error correction
- Trade-offs between energy dissipation and raw error rate.

Conclusions

- Silicon CMOS logic will be extended at least another 10 years.
  - New materials and transistor structures
  - Cooperative circuit and device technology co-design
- BUT … we appear to be entering an era in which fundamental physics and truly adventurous electrical engineering can again play a central role in the evolution of information technology.

Thanks to colleagues ...

Paul Solomon

David J. Frank

Charles Bennett

Bob Keyes

and Roger Koch (deceased)

for many discussions, both recent and long past ...

… and thanks for your attention!