

Extreme Hardware

“Extreme”

Definition: *very great*

Synonyms: *...consummate, great, greatest, high, highest, intense, maximal, maximum, severe, sovereign, supreme, top, ultimate...*

Definition: *unreasonable*

Synonyms: *...desperate, dire, downright, drastic, egregious, exaggerated, exceptional, excessive, extraordinary, extravagant, fabulous, fanatical...*

Chairman's Note: This document was prepared by the “extreme hardware” working group and was received by the entire workshop in plenary session without modification.

Moore's Law

...2 years...

...18 months...

...clock speed...

...transistor...

...performance...

...17%...

...50%...

“The complexity for minimum component costs has increased at a rate of roughly a factor of two per year”

<http://arstechnica.com/articles/paedia/cpu/moore.ars>

Interesting quotes

.No one has taken reversible computing seriously, no significant funding at all.

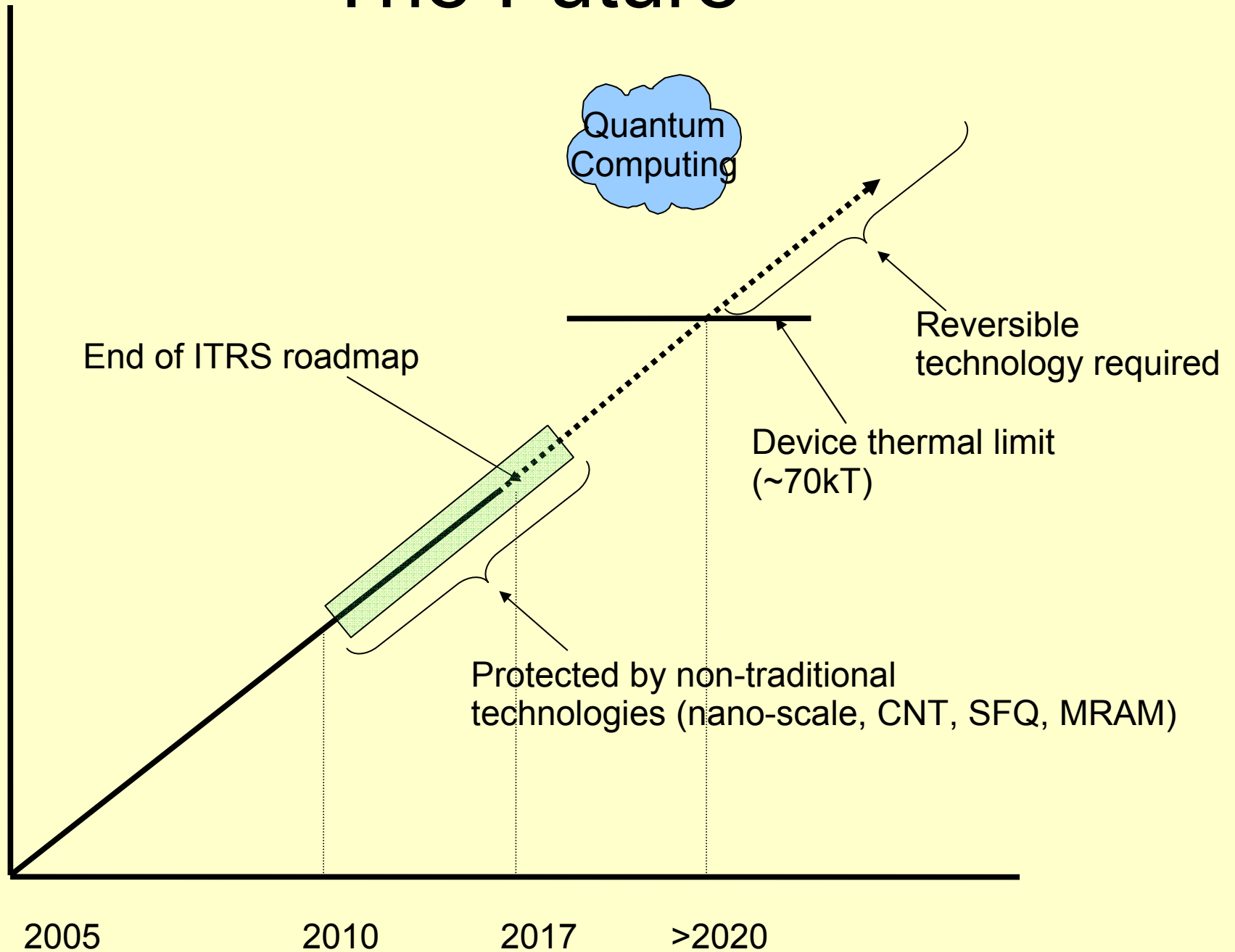
.Reversible SFQ....interesting combination.

.What do the nano-technologies do to the programming model?

.Should legacy code be considered?

.Successor technologies will likely be evolutionary rather than revolutionary technologies that can use CMOS litho, processes, or investments.

The Future



Results

.No issues with CMOS for next 5 years, billion dollar market creates huge momentum and justification to invest in R&D.

.Between 5 and 12 years out, there is some risk in CMOS providing exponential performance gains, but this risk is well mitigated by several classes of promising technologies; nano-scale lithography and architectures, carbon-nano-tube memory, MRAM, and SFQ.

Between 15 and 20 years out, device thermal limit creates a floor for classic device architecture, the only known long term solutions past this floor are Reversible logic and Quantum Computing.

Results

Group agreed to do two things:

- 1) Create and complete a matrix of characteristics and metrics for each technology.
- 2) Architect a toy requirement and implement a solution in each technology, eg a 'contest'.

Technology characteristics and metrics

.Application space

.Technical Risk

***.Performance (measured by operations/Joule-sec),
for each of:***

. processor

. interconnect

. memory

OR

. compute ability

.Market feasibility

.Investment needed to prototype

.Scalability

.Number of Parties Developing

.Programming model

Contest (need more benign word)

- .Need a requirement, not an architecture.***
- .Needs to represent some of the metrics in the previous matrix***

.Possibilities discussed:

- . Factoring***
- . Simple ALU***

Other thoughts

.We need to advertise that the future does not hold 'A' replacement for the transistor, and that future solutions will be heterogeneous.

- . Signs of a heterogeneous solution are already occurring for interconnect and memory solutions.***

.Assuming 50% increase in performance every 2-years, we would need an additional 10^3 performance increase to get to Zetta-Flops by 2020.

Other thoughts

Technological walls may not be the only problem for US HPC vendors. In 10 years, the capitol investment costs needed will force the reduction of US fabs: Intel, IBM, Freescale, TI, LSI Logic