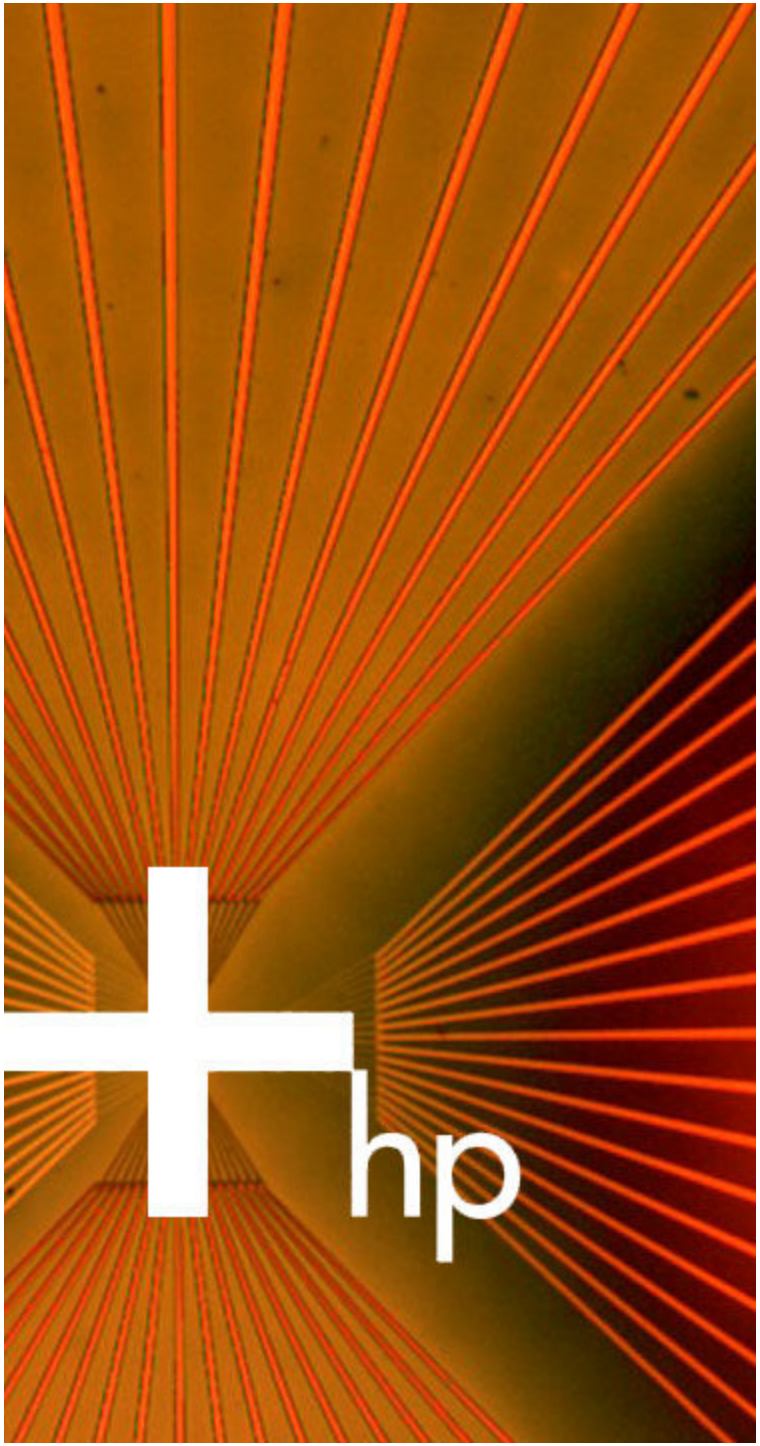
Manufacturability and Computability at the Nano-Scale

Frontiers of Extreme Computing



Stan Williams
October 25, 2005

"The purpose of QSR is to perform fundamental research in physical science with a strategic intent for hp – to create new technologies that will be important to the company on a 10+ year time frame."

Discover + Invent

For a more detailed discussion of this work, see

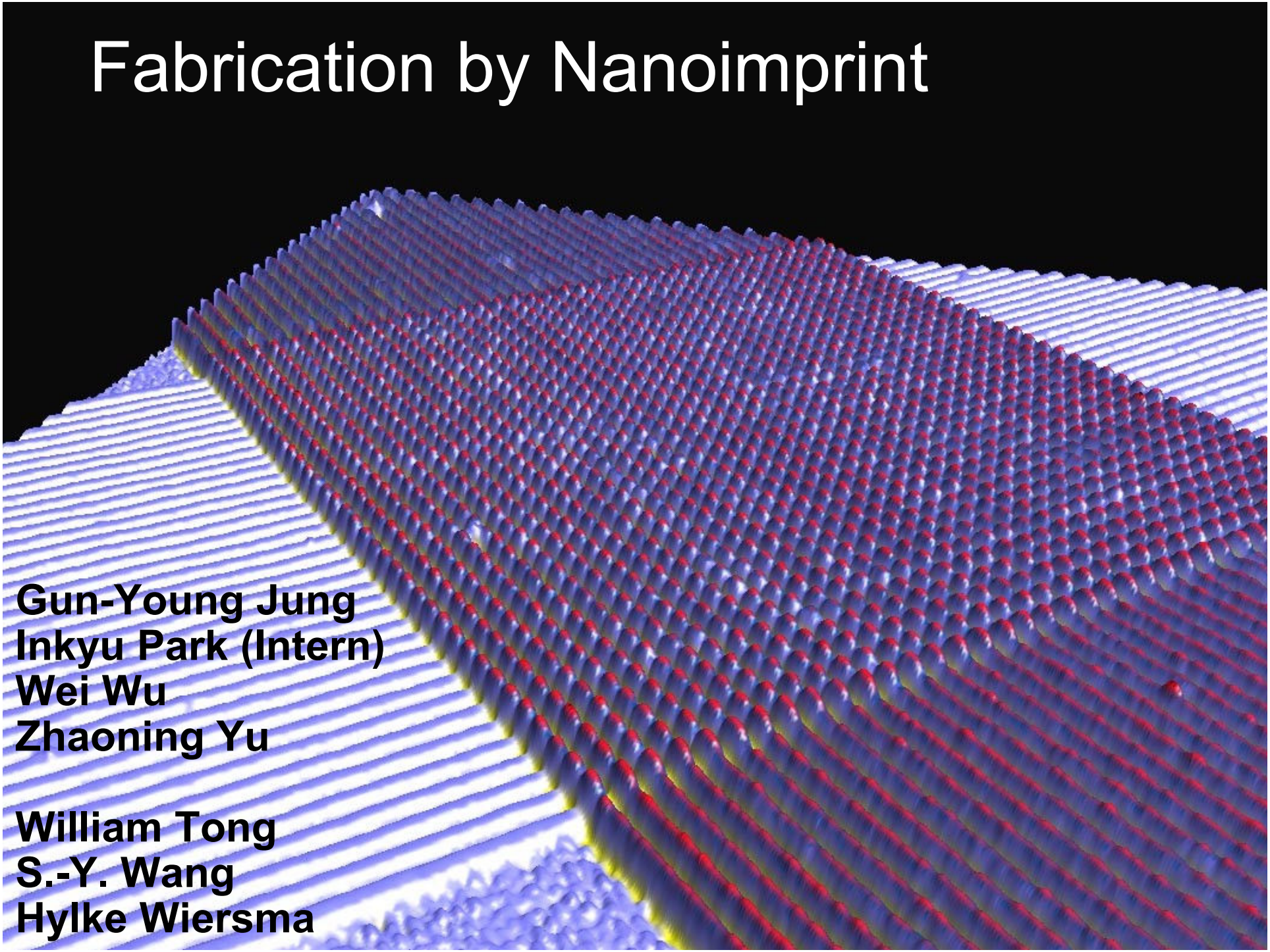
Applied Physics A **80**, March 2005

"Nanoelectronics" Special Issue

Journal of Applied Physics 97, #034301 (2005)

2005 WSJ Technology Innovation Award

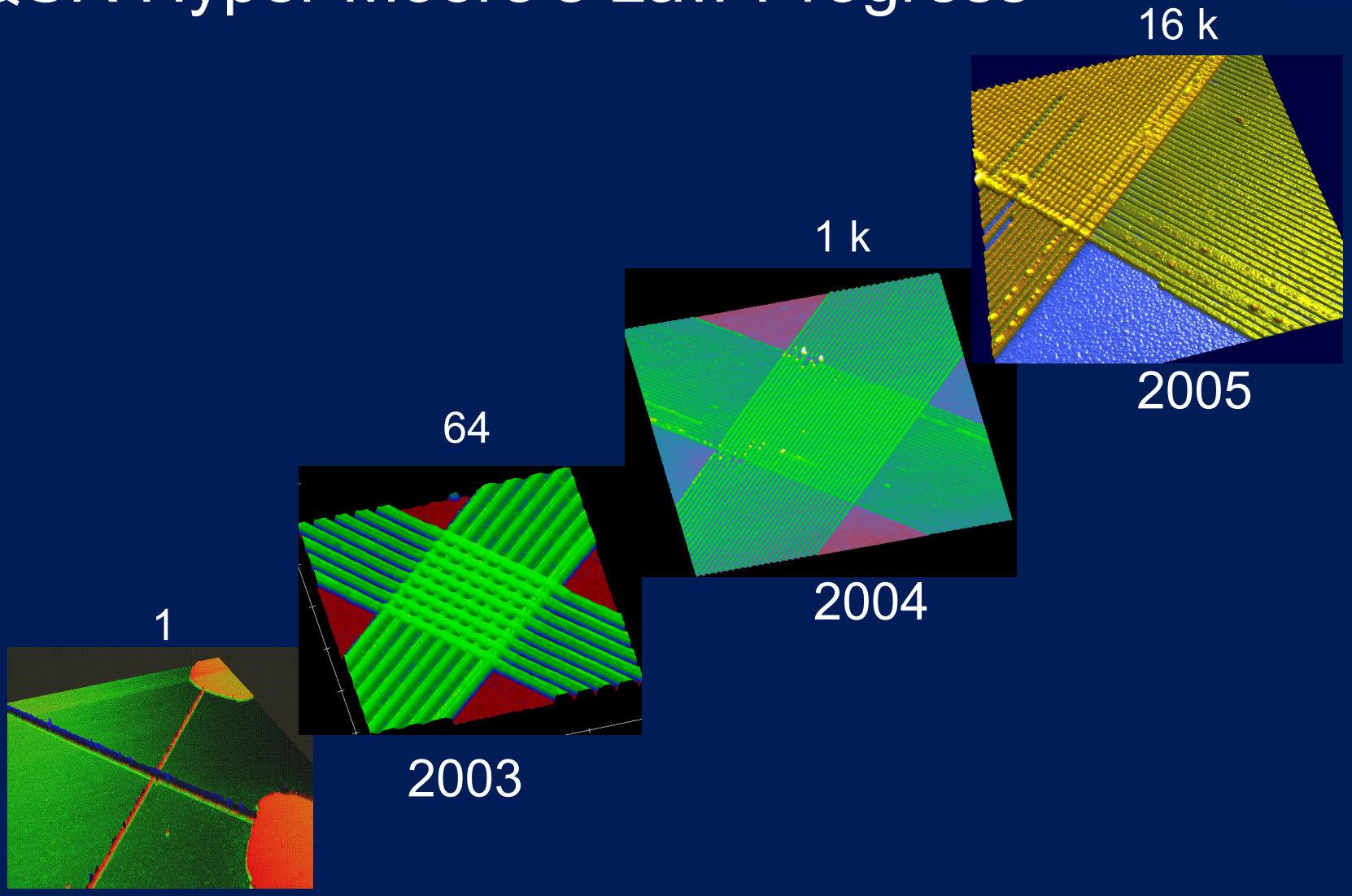
Fabrication by Nanoimprint



Gun-Young Jung
Inkyu Park (Intern)
Wei Wu
Zhaoning Yu

William Tong
S.-Y. Wang
Hylke Wiersma

QSR Hyper Moore's Law Progress



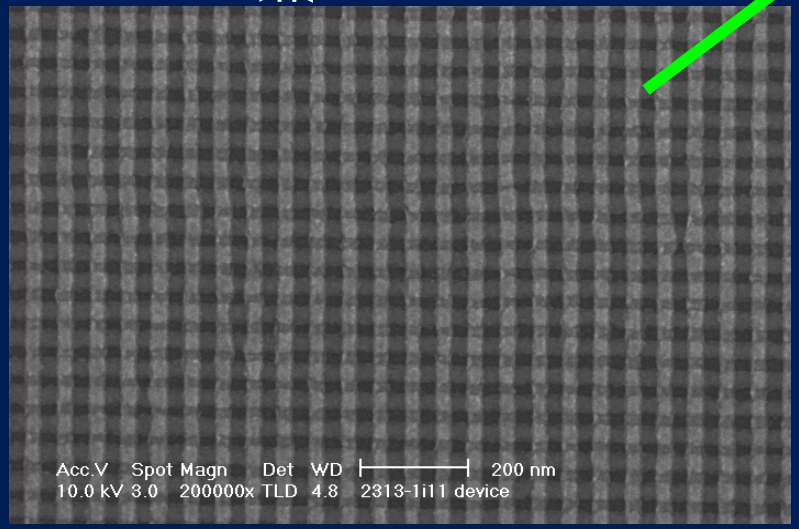
Lithography Red Brick Wall - 2010

QSR > 13 years ahead!

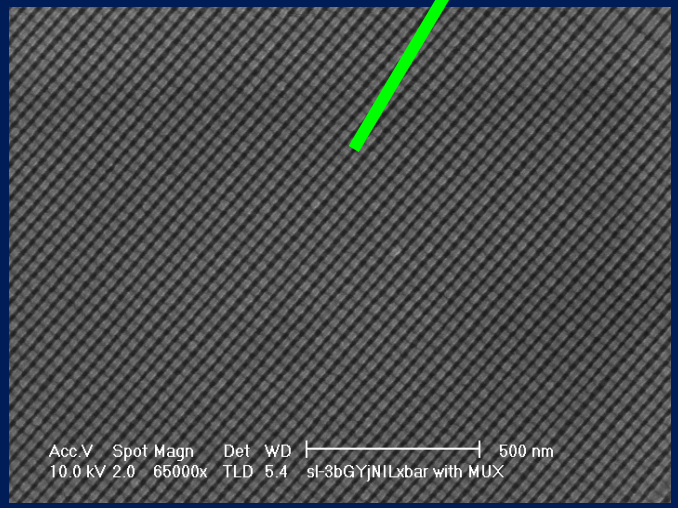
International Technology Roadmap for Semiconductors 2004

year	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18
DRAM ½ pitch nm	90	80	70	65	57	50	45	40	35	32	28	25	22	20	18

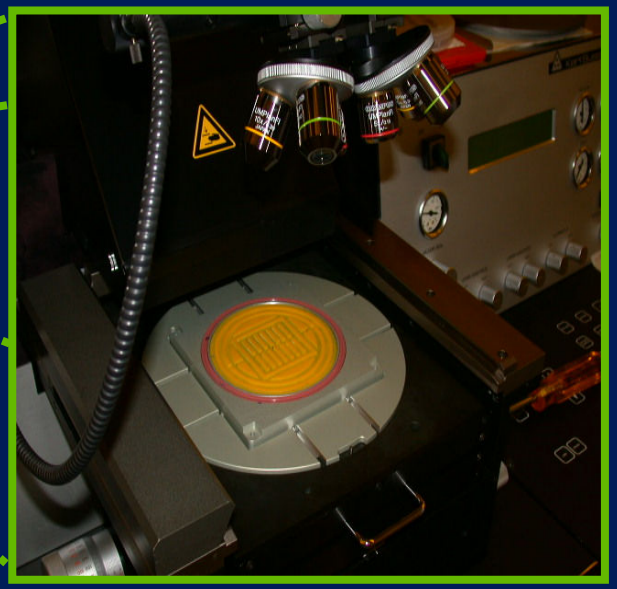
30 nm

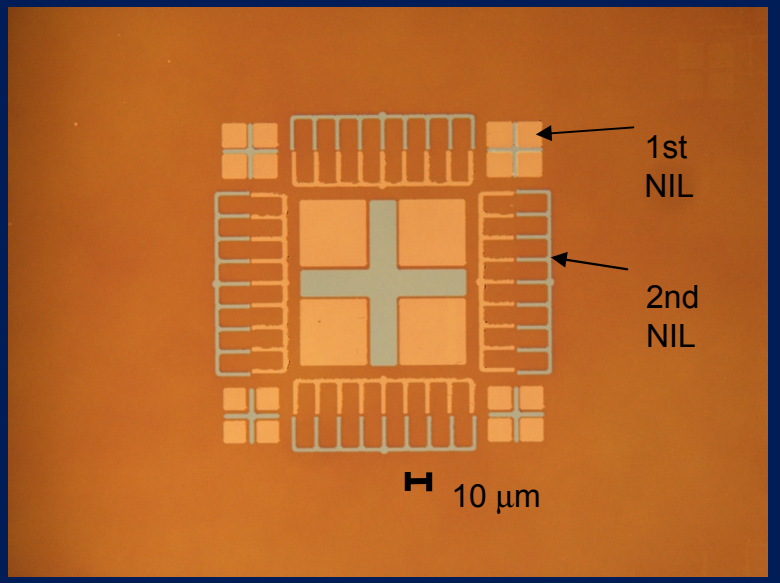


17 nm



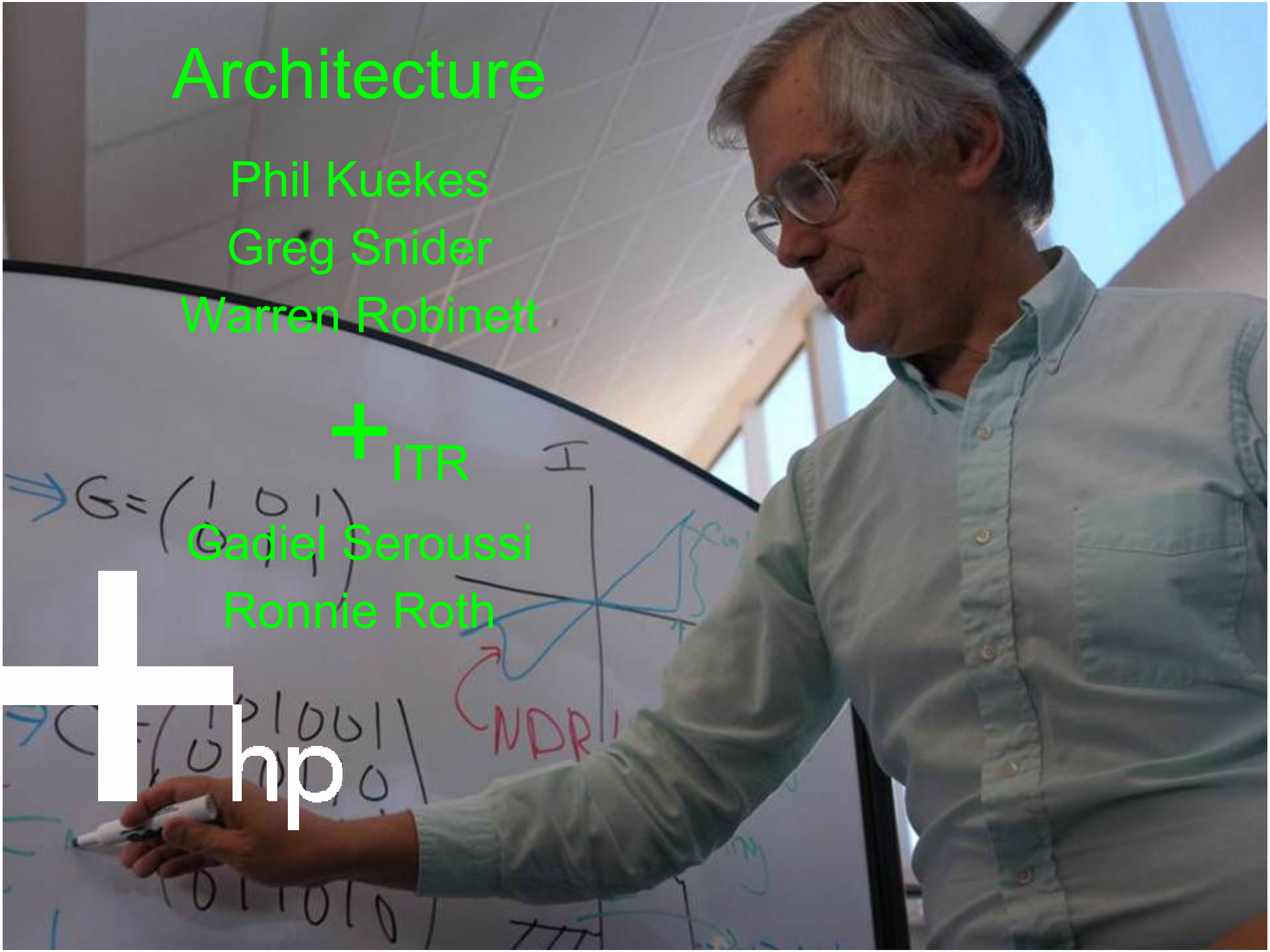
G4 nanoimprinter: Total cost $300k





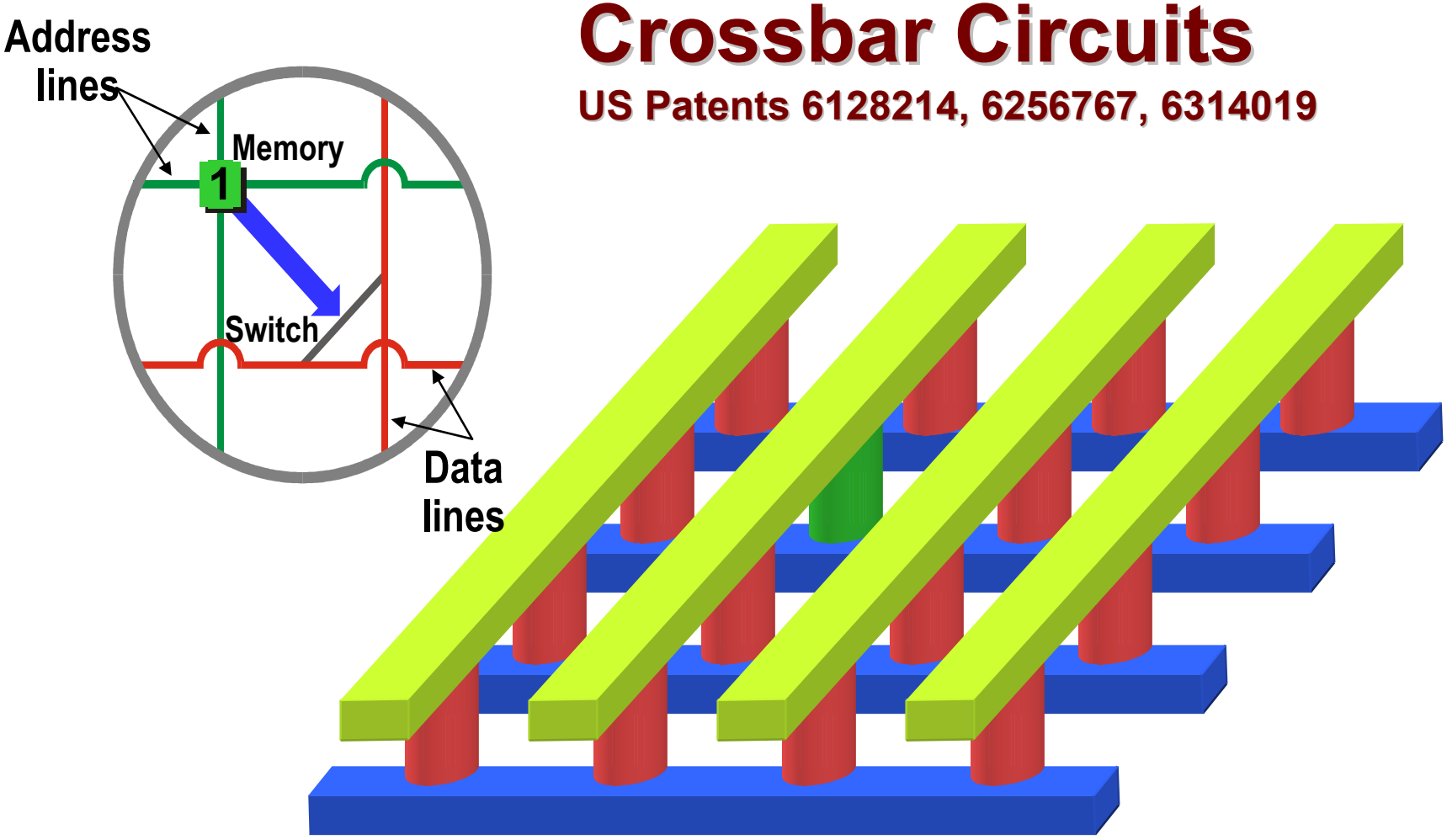
Wei Wu

- Much more cost-effective than any commercial nanoimprinter
- 0.5 μm alignment accuracy demonstrated
- Targeting 10 nm alignment accuracy (with J. Gao & C. Picciotto)
- Step & repeat compatible design


Architecture
Phil Kuekes
Greg Snider
Warren Robinett
+ ITR
Gadiel Seroussi
Ronnie Roth
+ hp

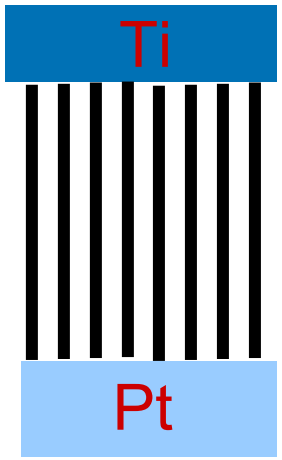
Tunneling-Switch Crossbar Circuits

US Patents 6128214, 6256767, 6314019

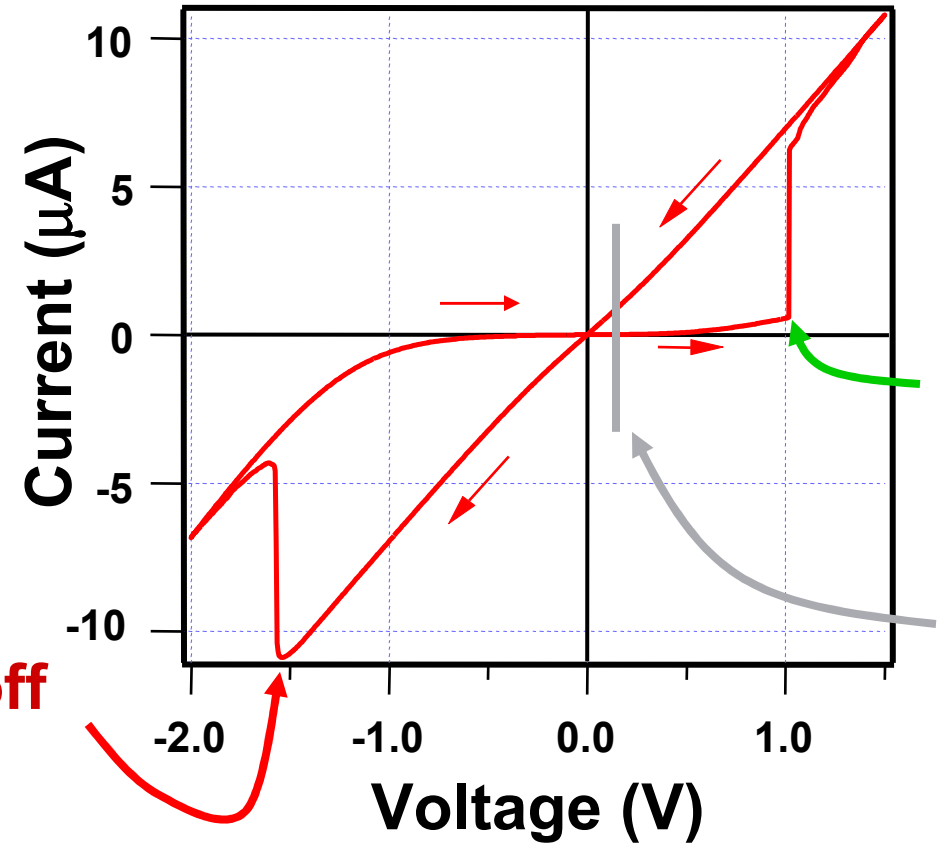


Abstraction of a Field-Programmable Gate Array

Switchable Tunneling Resistor



Device =
Molecule
+ Electrodes

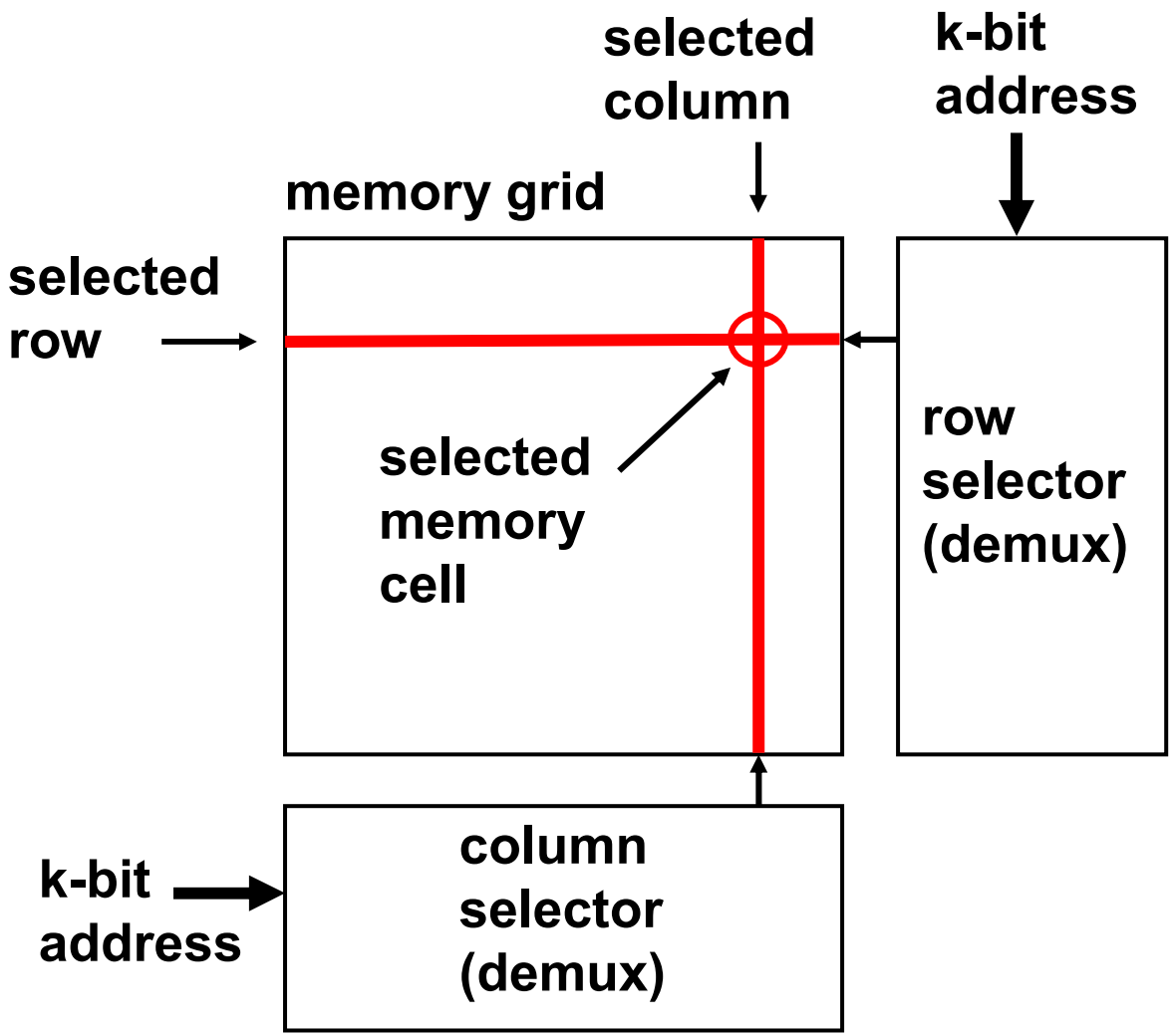


Switch on "1"

Read bit (measure resistance)

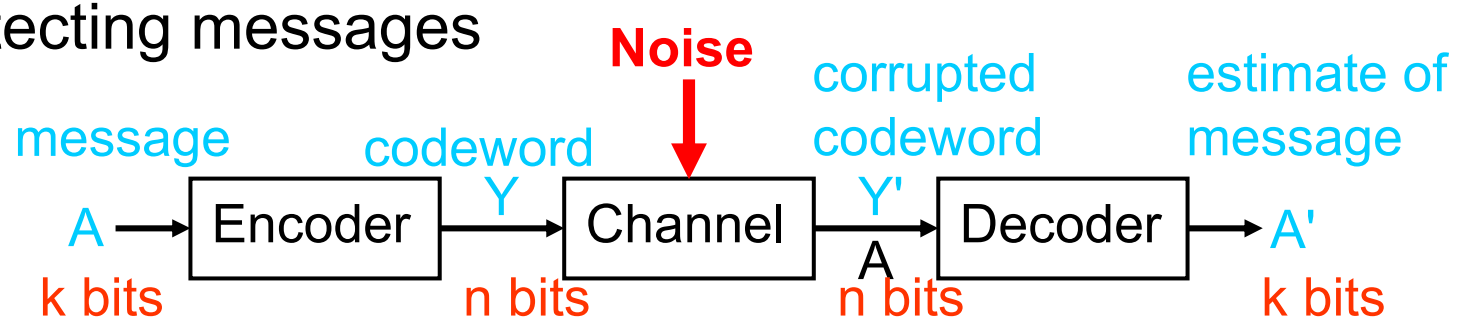
Switch off "0"

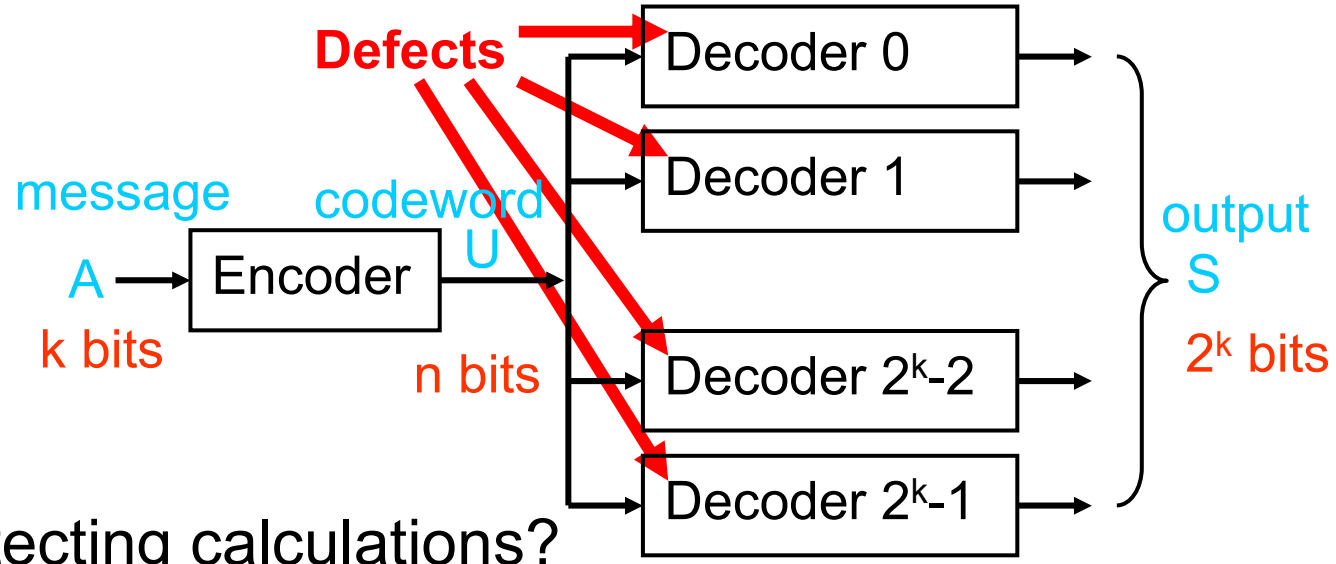
Communicate with the nanowires



Use coding theory to design circuits!

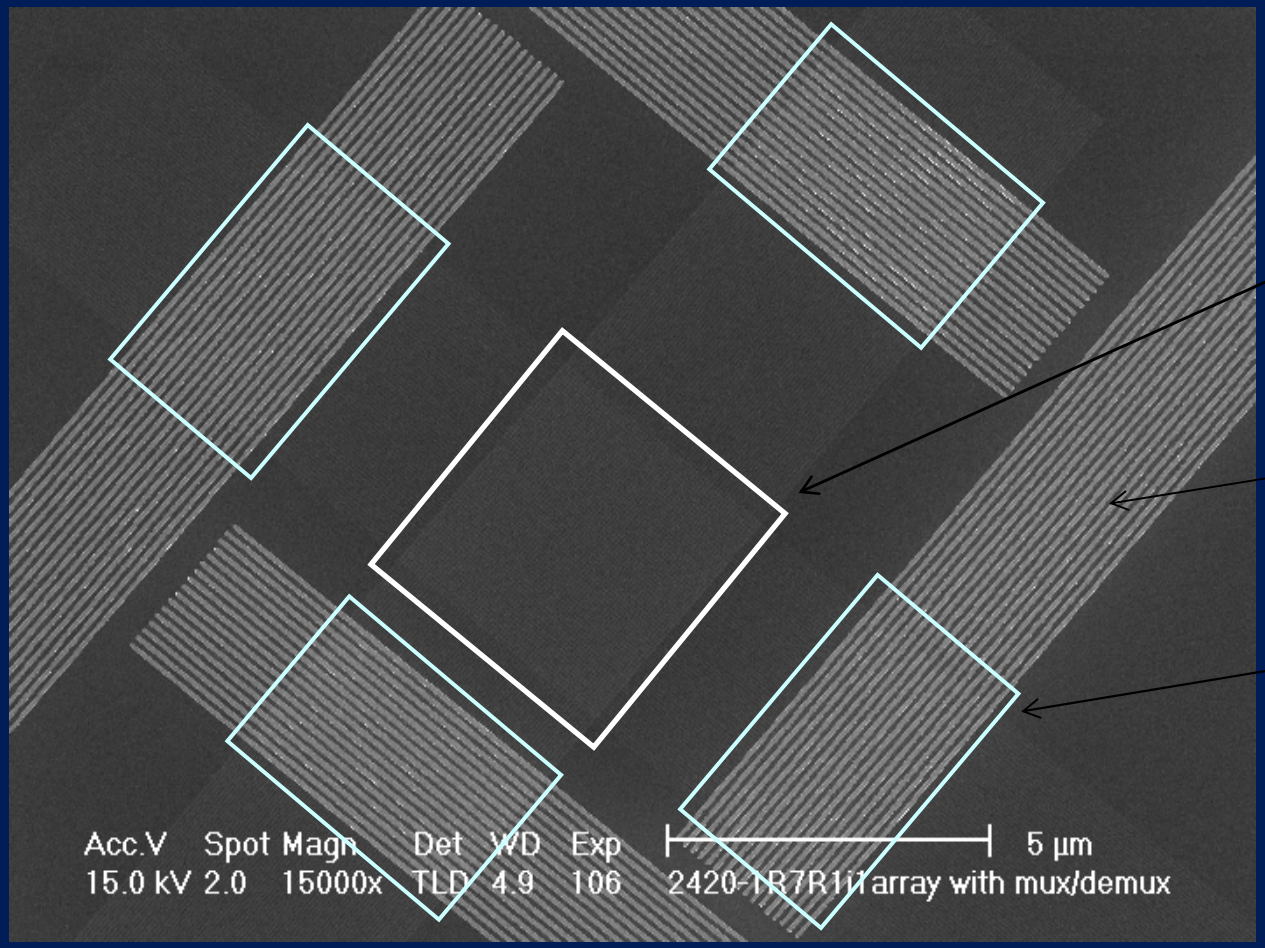
- Protecting messages





Protecting calculations?

Four kbit Cross Bar Memory with Mux/Demux

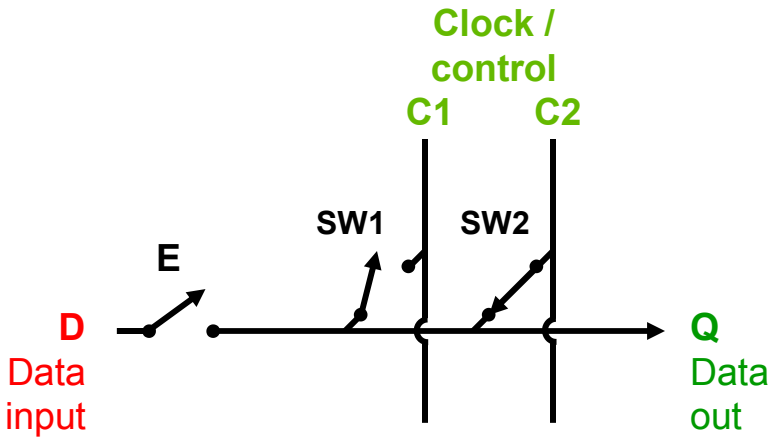


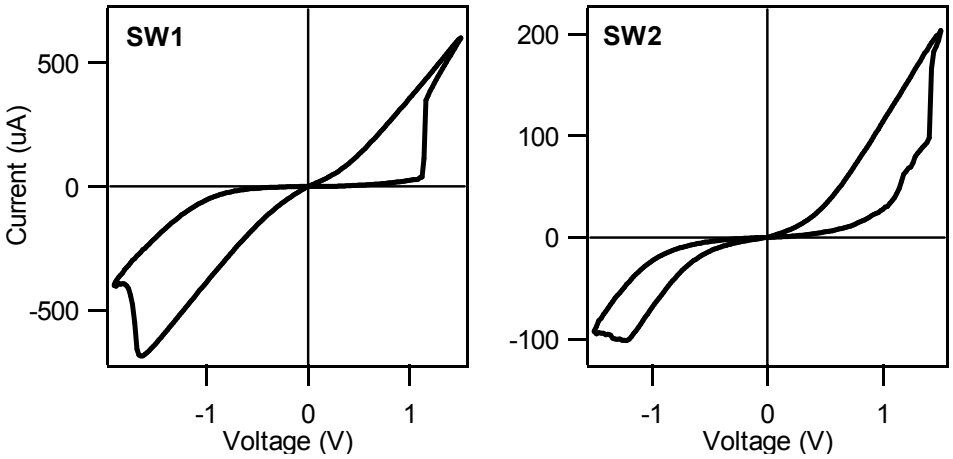
*Mux/demux propramming done by E-beam burning

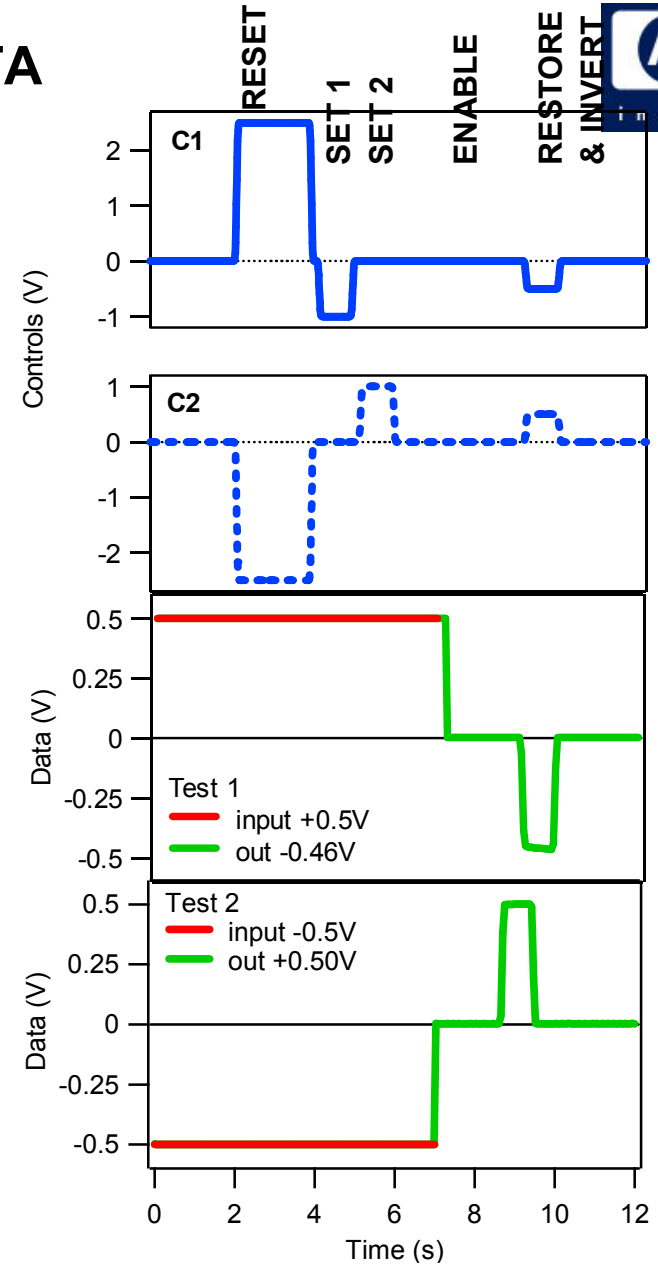
No Gain,

No Logic?

TUNNELING SWITCH LATCH: EXPT DATA

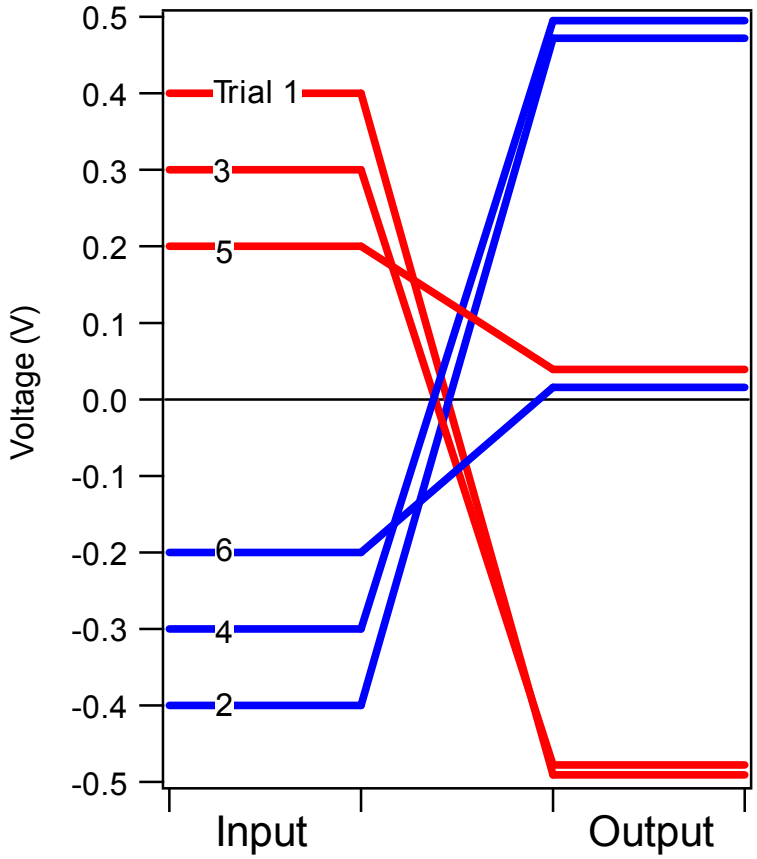






Duncan Stewart

Expt: *Latch works!*



Signal restoration

Inversion, if desired

>100mV operating margin

No nanoscale transistor!

J. Appl. Phys. Feb 1, 2005

The Tunneling-Switch Latch Provides

Logical State Storage

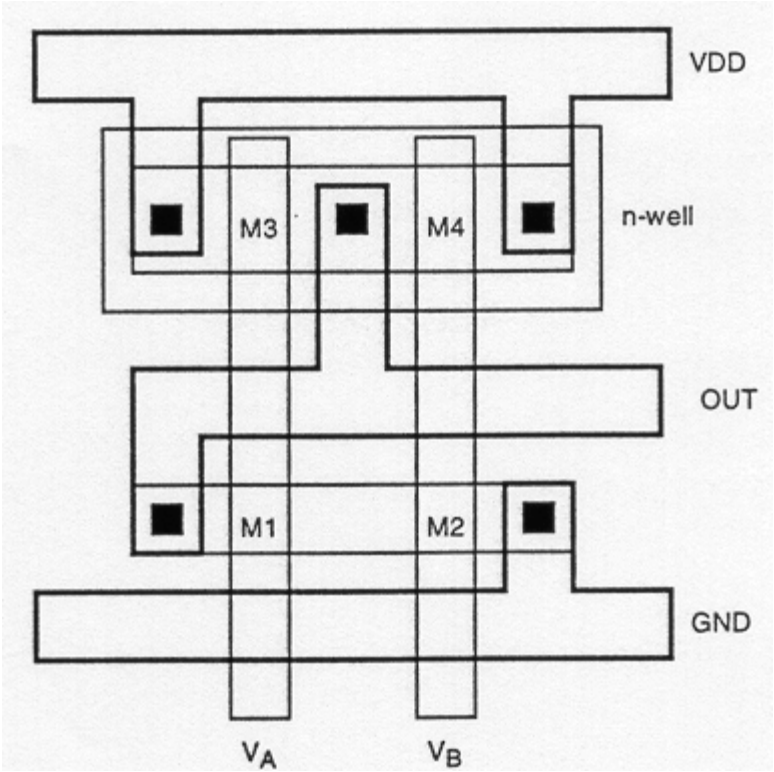
Signal Restoration

Signal Inversion (Logical NOT)
(with no need for a nanoscale transistor)

Universal Computation!
(Finite State Machine with wired ANDs and ORs)

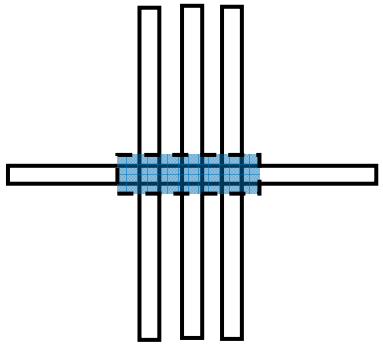
Area comparison of NAND gates

CMOS NAND gate



Area = 36×(FP)^2
= 1.2μ^2 @ 90 nm hp

SIMPL NAND gate



Area = 3×(FP)^2
= 0.01μ^2 @ 30 nm hp

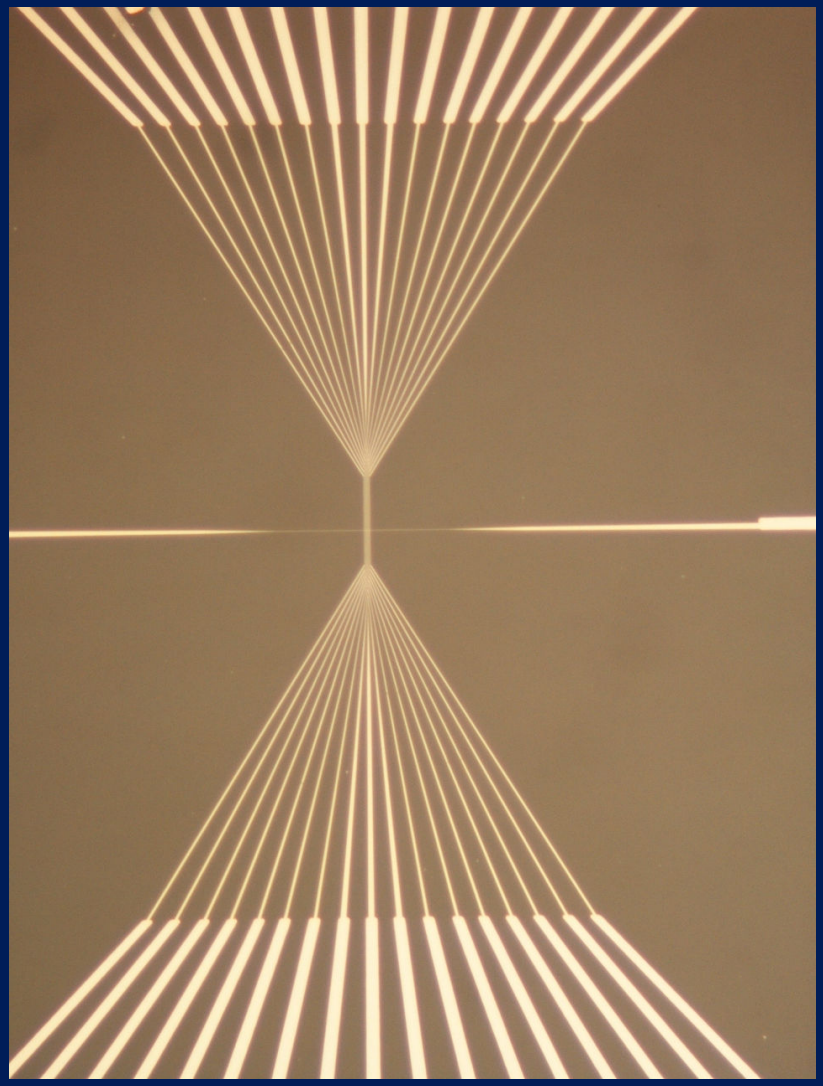
No V_{DD}, no static power!

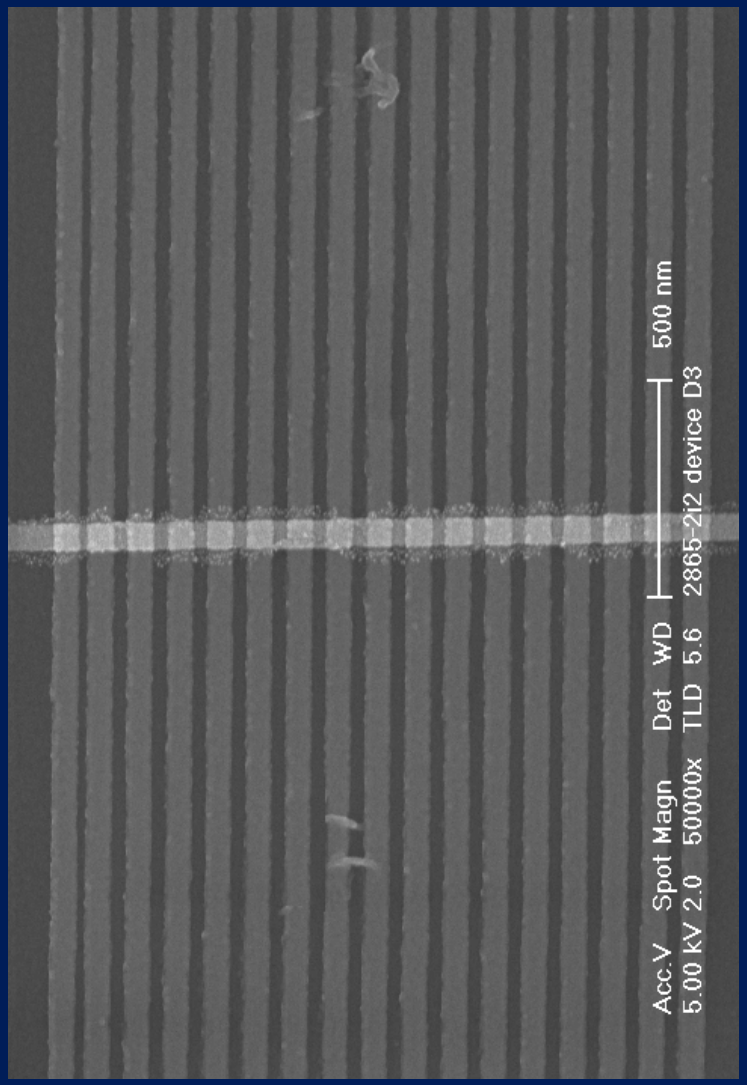
Low dynamic power

Register and Logic

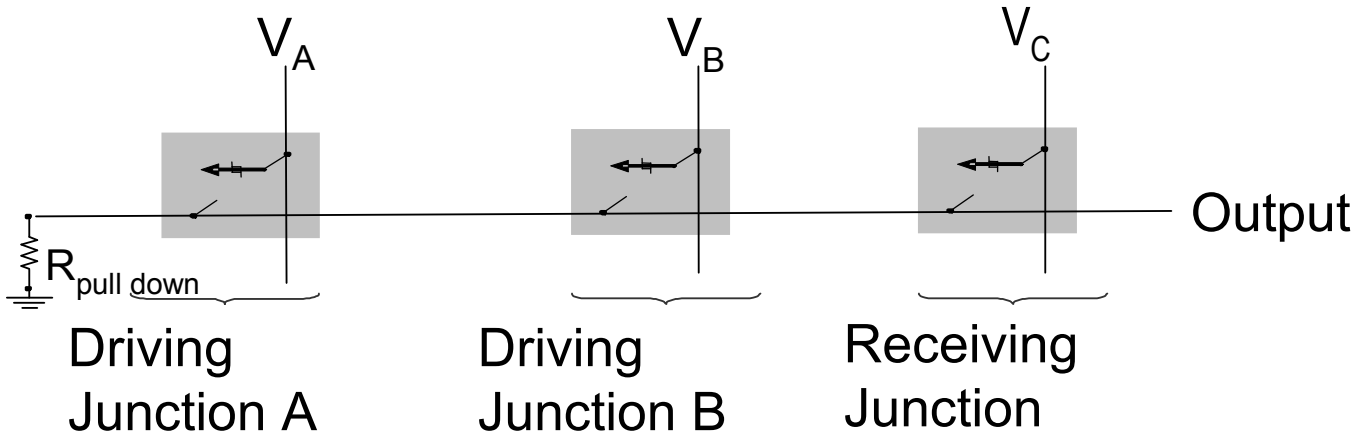
Permute inputs and outputs

1 x 17 Latch and Logic Array





Experimentally measured NAND truth table – Output on $R_{pull\ down}$ measured at indicated Step



Junction A	Junction B	$R_{pull\ down}$	Step #
0	0	1	10
0	1	1	19
1	1	0	28
1	0	1	37

Experimental V vs. t data for NAND demonstration

Summary of Serial Implication Logic

- SIMPL is simple!
- Tunneling switches ➔ *state machines*.
- Linear array + demux; high density.
- State encoded with impedance, not voltage.
- No static power dissipation.
- Nonvolatile.
- Conditional copy with inversion is ‘implication’
- Compiler construction completed.
- nanoCircuits built and currently under test.


hp
invent