Workshop on the Frontiers of Extreme Computing

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Sandia National Laboratories

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Issues

- The 1994 meeting looked to the future
  - 100 Gigaflops × 10,000 → 1 Petaflops
- By contrast, this meeting has no numerical target
  - We have full range of applications represented
    - FLOPS + (some) non-FLOPS
  - We have hardware represented that can run the software, creating a balance
- Drama: we have a "phase change" in the realm at
  - 100 Petaflops for $100M leadership class supercomputer or
  - 1 Petaflops for $1M university class supercomputer

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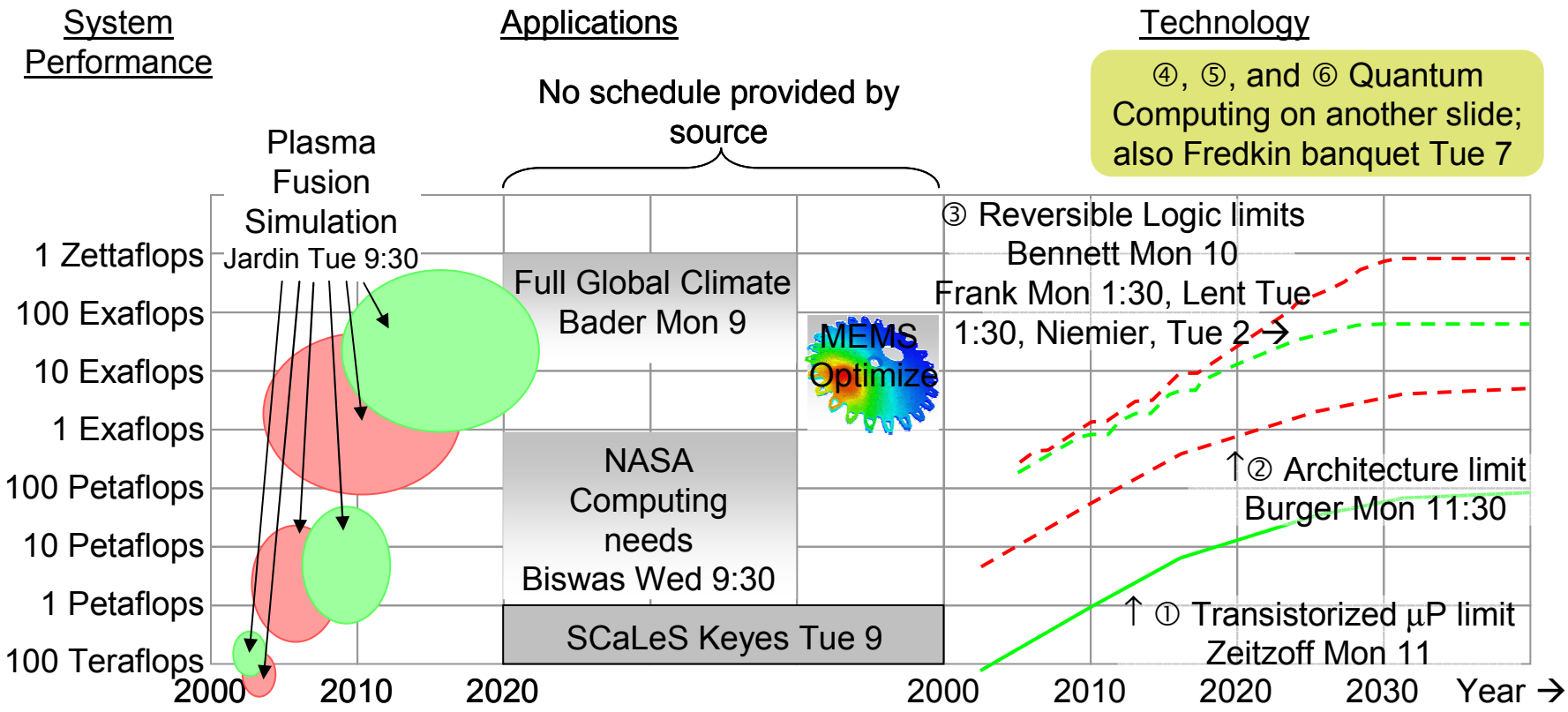
Applications and $100M Supercomputers



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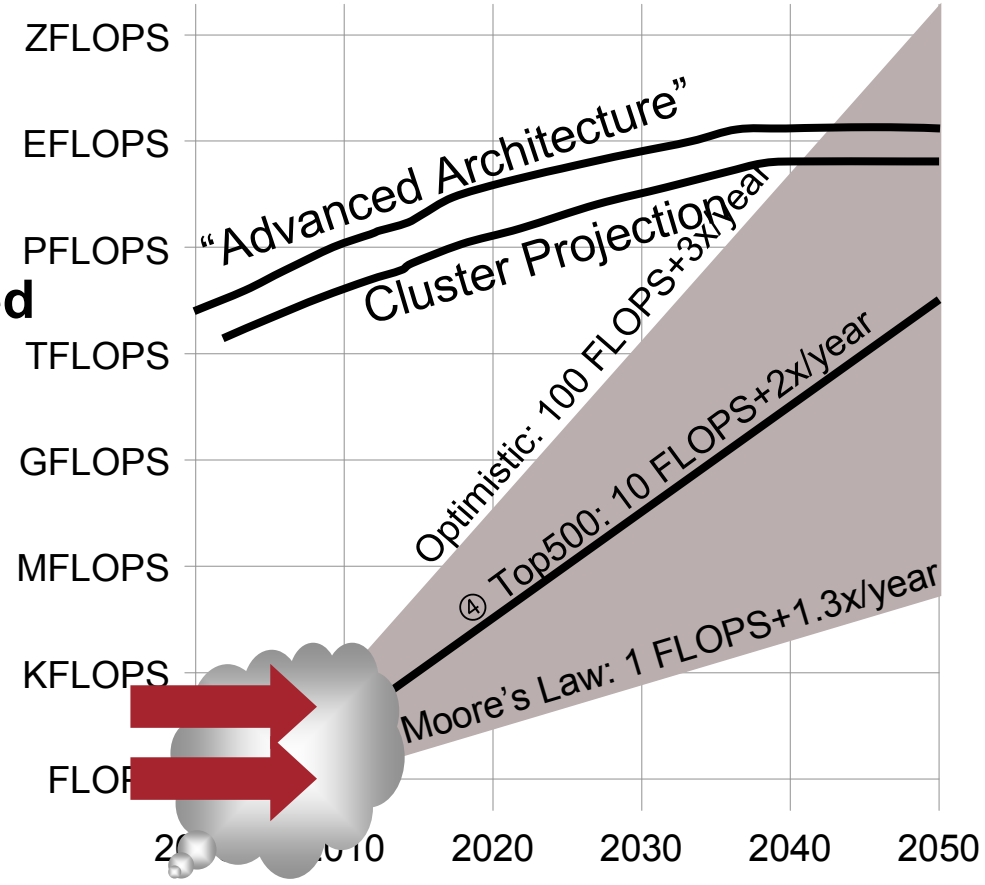
Emergence of Quantum Computing

- **Oskin Wed 2 PM has a paper on how to build a 1 FLOPS QC**
  - **delivery date unstated**
- **One would expect an exponential growth rate for quantum computers similar to Moore's Law, but the rate constant is impossible to predict, so three possibilities have been graphed**



Note: I don't have anything to say about <u>when</u> the first practical QC will be built. This will not affect the argument. Hence "cloud."

Ref. "An Evaluation Framework and Instruction Set Architecture for Ion-Trap based Quantum Micro-architectures," Steven Balensiefer, Lucas Kregor-Stickles, and Mark Oski, University of Washington

"How to build a 300 bit, 1 Gop quantum computer," Andrew M. Steane, Clarendon Laboratory, UK, quant-ph/0412165

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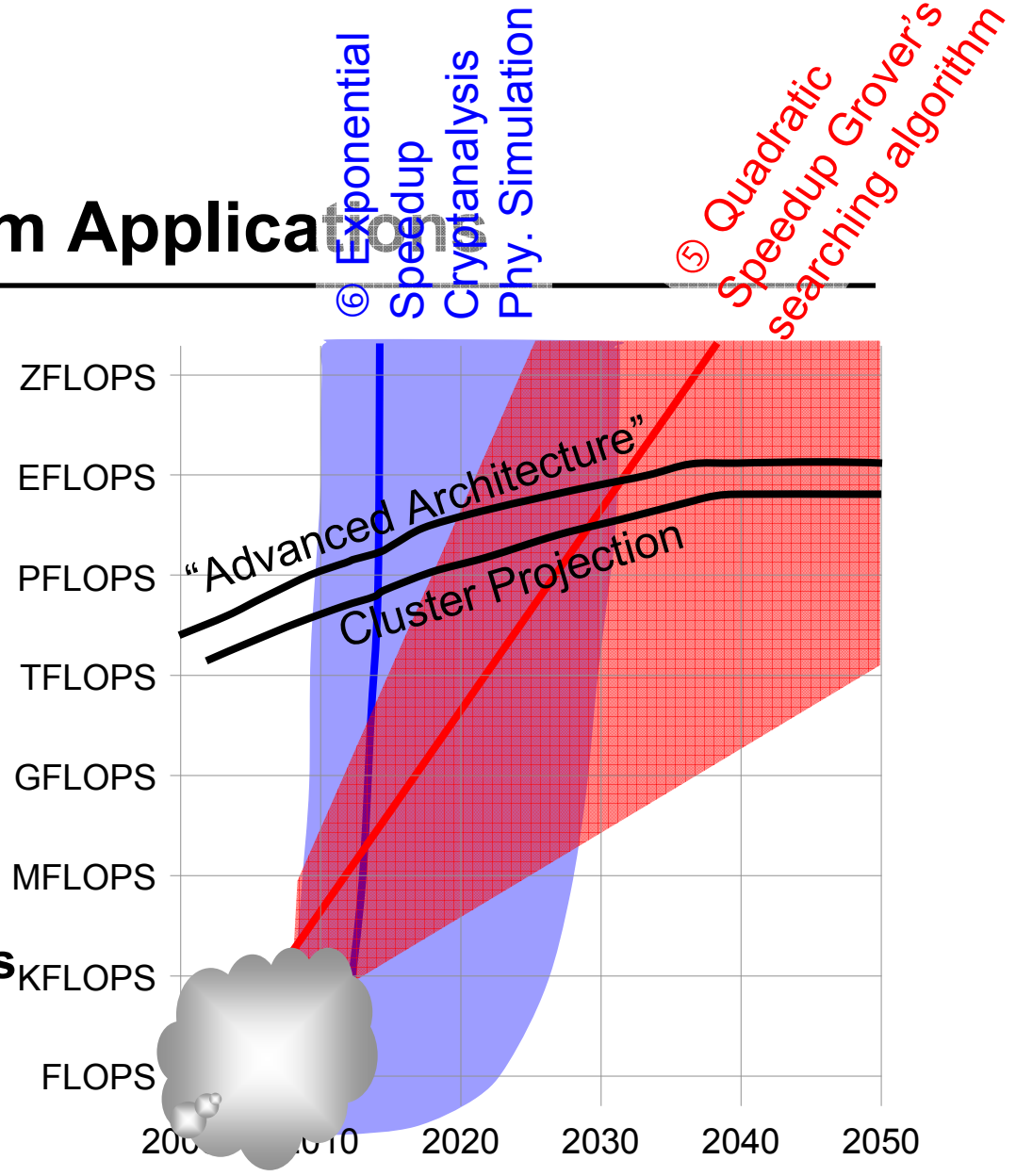
Quantum Applications

- **Consider the classical computer equivalent to a Quantum Computer**
- **Williams Wed 2:30 will discuss physical simulations with exponential speedup over classical (blue)**
- **Searching algorithms broadly parallelize loops and can achieve quadratic speedup over a classical computer**



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Hardware Questions

- Evolutionary Trends
  - What can we expect from transistors, nanotech, & superconducting in current class of computation?
- Drive Current Computing Class to Maturity
  - How can we optimize architectures (mostly for power) in order to get a final 100× performance boost before flat lining?
- Move to the Next Computing Class
  - Should reversible logic and/or quantum computing be considered for the mainstream?

Applications and Software Questions

- Applications
  - How strong is the case for building big computers to solve important problems?
  - Can we better synchronize hardware roadmaps with applications plans
- Software
  - ALL classical (non-quantum) computing options involve dramatic increase in parallelism
  - There is virtually nobody looking into how algorithms and programming
  - Other issues

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ITRS Emerging Research Devices (2004)

- Seeks research options for long term continuation of Moore's Law
- Table ↘ created by tallying votes of a committee of industry "experts."
- Color codes, likely, possible, unacceptable

Table 67 Technology Performance and Risk Evaluation for Emerging Research Logic Device Technologies (Potential/Risk)

Logic Device Technologies (Potential/Risk)	Performance [A]	Architecture compatible [B]*	Stability and reliability [C]	CMOS compatible [D]**	Operate temp [E]***	Energy efficiency [F]	Sensitivity Δ(parameter) [G]	Scalability [H]
1D Structures	2.3/2.2	2.2/2.9	1.9/1.2	2.3/2.4	2.9/2.9	2.6/2.1	2.6/2.1	2.3/1.6
RSFQ Devices	2.7/3.0	1.9/2.7	2.2/2.8	1.6/2.2	1.1/2.7	1.6/2.3	1.9/2.8	1.0/2.1
Resonant Tunneling Devices	2.6/2.0	2.1/2.2	2.0/1.4	2.3/2.2	2.2/2.4	2.4/2.1	1.4/1.4	2.0/2.0
Molecular Devices	1.7/1.3	1.8/1.4	1.6/1.4	2.0/1.6	2.3/2.4	2.6/1.3	2.0/1.4	2.6/1.3
Spin Transistor	2.2/1.7	1.7/1.6	1.7/1.7	1.9/1.4	1.6/2.0	2.3/2.1	1.4/1.7	2.0/1.4
SETs	1.1/1.2	1.7/1.2	1.3/1.1	2.1/1.4	1.2/1.8	2.6/2.0	1.0/1.0	2.1/1.7
QCA Devices	1.4/1.3	1.2/1.1	1.7/1.8	1.4/1.6	1.2/1.4	2.4/1.7	1.6/1.1	2.0/1.4

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Emerging Research Devices (notes 2005)

- Notes from 2005 meeting
- Immediate implication: all devices unacceptable except CNFET
- However CNFET is a short term solution, and belongs on a different table

> 20	>16 - 18
>18 - 20	≤ 16

For each Technology Entry (e.g. 1D Structures, sum horizontally over the 8 Criteria
Max Sum = 24
Min Sum = 8

Evaluation of Emerging Research Logic Device Technologies against Technology Evaluation Criteria

Logic Device Technologies	Scalability	Perform-ance	Energy Efficiency	Gain	Operational Reliability	Room Temp. Operation ***	CMOS Compatibility **	CMOS Architectural Compatibility *
1D Structures	2.4	2.4	2.1	2.4	2.3	2.9	2.4	2.6
Resonant Tunneling Devices	1.4	2.0	1.9	1.7	1.7	2.9	2.1	2.1
SETs	1.9	1.0	2.5	1.3	1.2	1.9	2.4	2.0
Molecular Devices	1.9	1.1	2.0	1.1	1.3	2.6	1.9	1.6
Ferromagnetic Devices	1.5	1.2	1.8	1.5	1.8	2.2	1.5	1.8
Spin Transistor	1.7	1.7	2.2	1.5	2.0	2.2	1.7	1.8

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