Inversion for S2LAL

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Abstract

This brief technical note is in response to the recently introduced S2LAL[1] reversible logic family, which is a static version of the 2LAL family.[2] I created inversion for 2LAL in a previous report,[4] and create inversion for S2LAL here using similar principles. S2LAL as described in ref. 1 requires quad-rail logic because there is no other source of inversion. Quad-rail logic is not necessary with the inversion in this note, although it can still be used. The availability of inversion will result in much smaller circuits in some cases.

S2LAL Inverter

Inversions in 2LAL and S2LAL follow the same principle. For 2LAL, I created a 2-level clock cascade, which had the disadvantage of extending the cycle from 4 to 6 ramps. However, S2LAL already contains an adequate 2-level cascade in the sense that ϕ_2 fits entirely within the flat top of S_1. In fig. 1, I repeat the method of using data signal S_1 in the 0 state to gate clock ϕ_2, which starts with the same shape as a 1 signal.

During forward clocking, each stage is expected to drive its output signal (S_2 or T_2) when ϕ_1 is high, making the transition from 0 to 1 (if there is to be a transition) at the same time as the ϕ_2 clock. The stage is expected to be tri-stated when ϕ_1 is low. The circuit in fig. 1 complies, thus creating $T_2 = -S_2$. As in ref. 4, this type of circuit runs backwards naturally and can be mirrored, so the method creates a new stream.

The intermediate signal Q_2 is created by using S_1 to select between ϕ_2 and ground. The timing diagram shows that the ϕ_2 clock transition occurs when the S_1 signal is stable, so Q_2 is a low-impedance voltage source and can deliver and recover energy.

The red circuitry in fig. 1 is shorthand for a pair of circuits with complementary voltages. All indices may be shifted, mod 8, allowing inversion to occur in any phase. The pass gate to a fixed voltage can sometimes be replaced by a single transistor, as in ref. 1.

In fact, the red circuitry in fig. 1a can be replaced by the two-input gates from ref. [1, figs. 8-9] as shown in fig. 1c, yet also allowing complemented inputs. Unlike 2LAL, signal inversion is permissible at this position in the circuit.

The enhancement in fig. 1 is not exactly an inverter; it takes a stream of bits and creates a second stream with the logical complement of the bits. The circuit can likewise create a new stream with the AND or OR of two input streams, including any combination of input inversions. Extension to XOR and XNOR is left as a future project.

Conclusions

This note shows that S2LAL may create new data streams from logical combinations of existing streams, including inverted terms. These streams can decomputed and the circuit will run backwards. Quad-rail circuitry is not needed, reducing overall complexity.

References

[1] Frank, Michael P., et al. "Reversible Computing with Fast, Fully Static, Fully Adiabatic CMOS." *arXiv preprint arXiv:2009.00448* (2020).

[2] V. Anantharam, M. He, K. Natarajan, H. Xie, and M. P. Frank. "Driving fully-adiabatic logic circuits using custom high-Q MEMS resonators," in *Proc. Int. Conf. Embedded Systems and Applications and Proc. Int. Conf VLSI (ESA/VLSI)*. Las Vegas, NV, pp. 5-11.

[3] *Enhancements to Adiabatic Logic for Quantum Computer Control Electronics*. Zettaflops LLC technical report ZF002, http://www.zettaflops.org/CATC/.

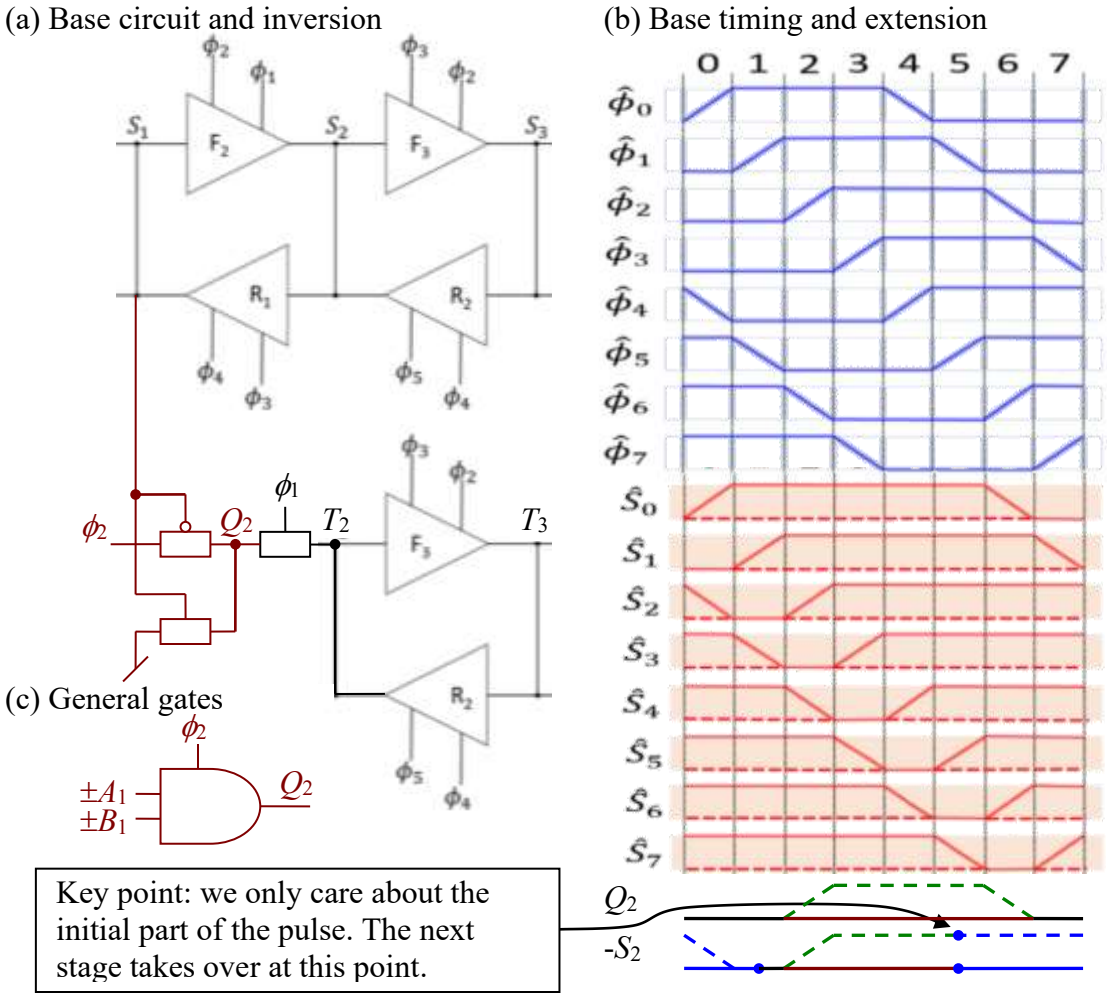

Fig. 1. S2LAL inversion. The (a) base circuit and (b) timing diagrams are copied from ref. 1, but I add three pass gates and the timing to invert the S_2 signal. The effect is not an inverter, but to launch an inverted stream $T_n = -S_n$. (c) Furthermore, the gates from [1, figs. 8-9] will work even with inverted inputs.