Cryogenic Adiabatic Transistor Circuits (CATC) for Quantum Computer Control

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(Based on WOLTE14 Presentation)

Summary

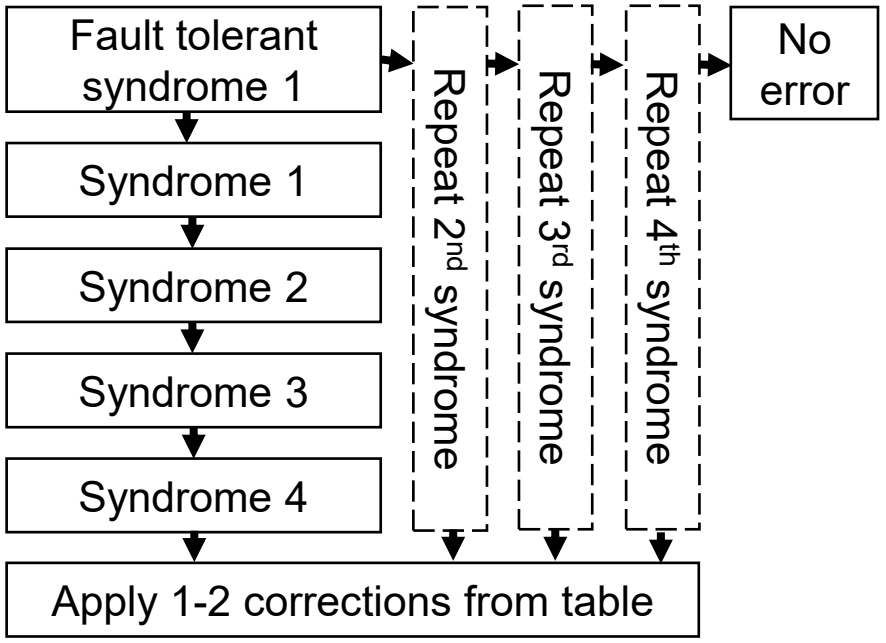
- Quantum computer scaleup is limited by the dissipation of classical electronics.* Digital addressed in this talk
  - CMOS means (1) transistors and (2) a circuit
  - Idea: Frank's S2LAL at cryo temperatures → Q2LAL
- Benefits:
  - ~1/1,000 heat in the cryostat
  - Lower noise in terms of power/amplitude
  - Noise can be below qubit control frequencies
  - Example cryo FPGA hybrid (e. g. reconfigurable logic)
- See https://zettaflops.org/isrds
  - These slides; full paper with simulation code, more

* Ref. Intel Horse Ridge lists digital and analog power about the same

Use Case: Classical Control of Quantum Computers

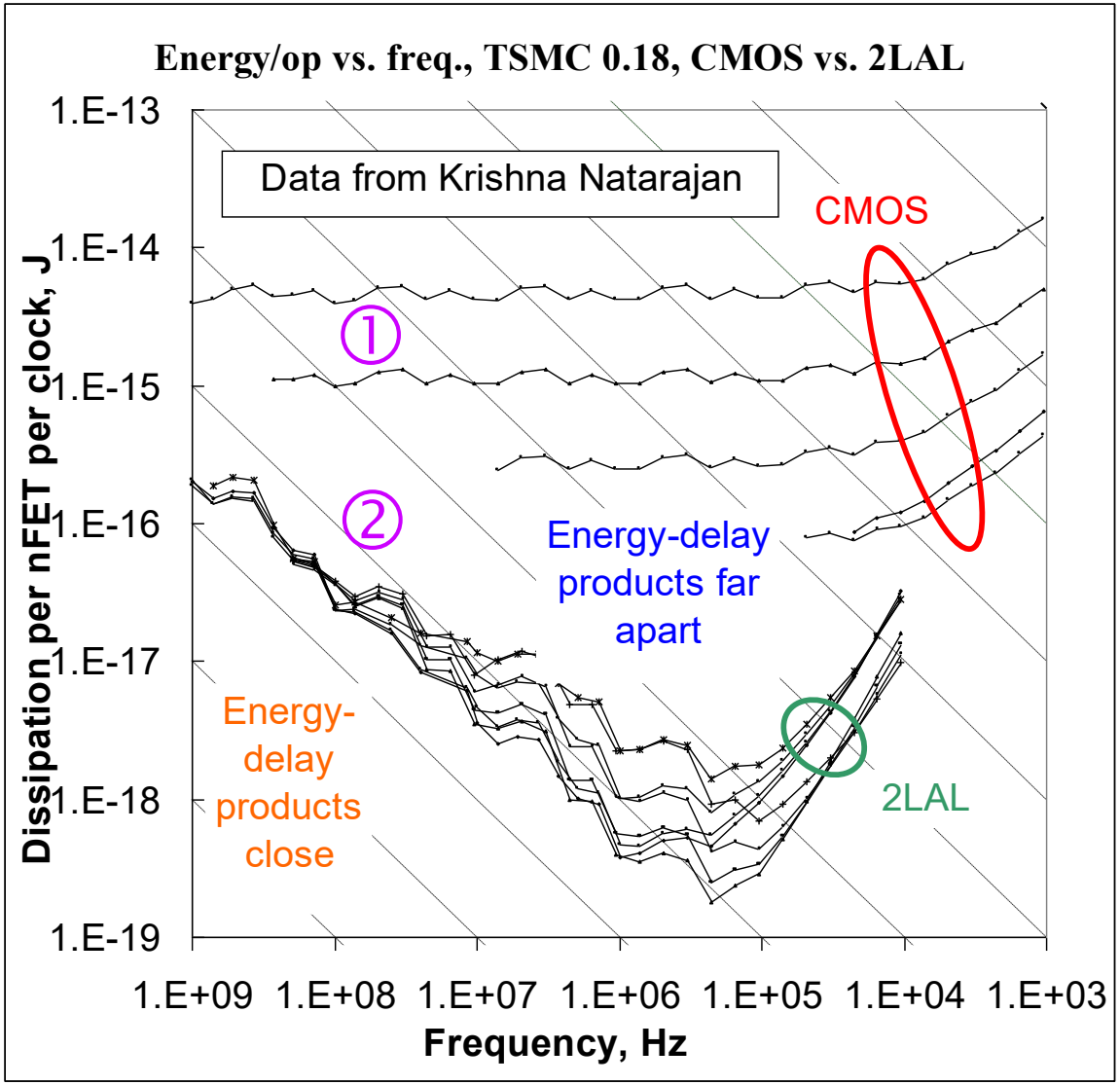
- Some classical functions should be near qubits
  - Set to |0> by measure and conditional NOT
  - Quantum error correction
  - Magic state factories
- Example
  - Classical automata with 4 branches and a look-up table
  - Blocks 1-2 dozen gates
  - The number of auto-mata scales, but their complexity does not

5-bit code arXiv:1705.02329:



Adiabatic Circuits

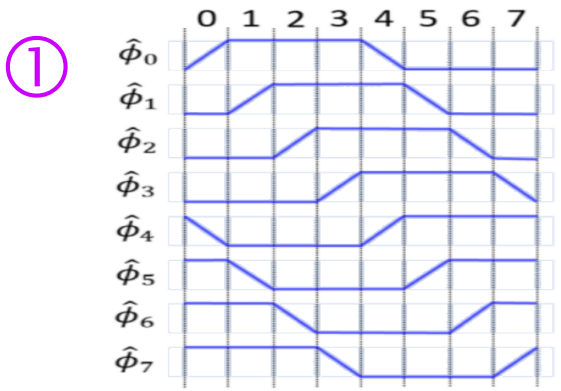
- Energy/op vs. clock period
- CMOS constant energy/op
- Adiabatic energy per op drops with clock period
- 1000× energy efficiency increase reasonable



Quiet 2 Level Adiabatic Logic

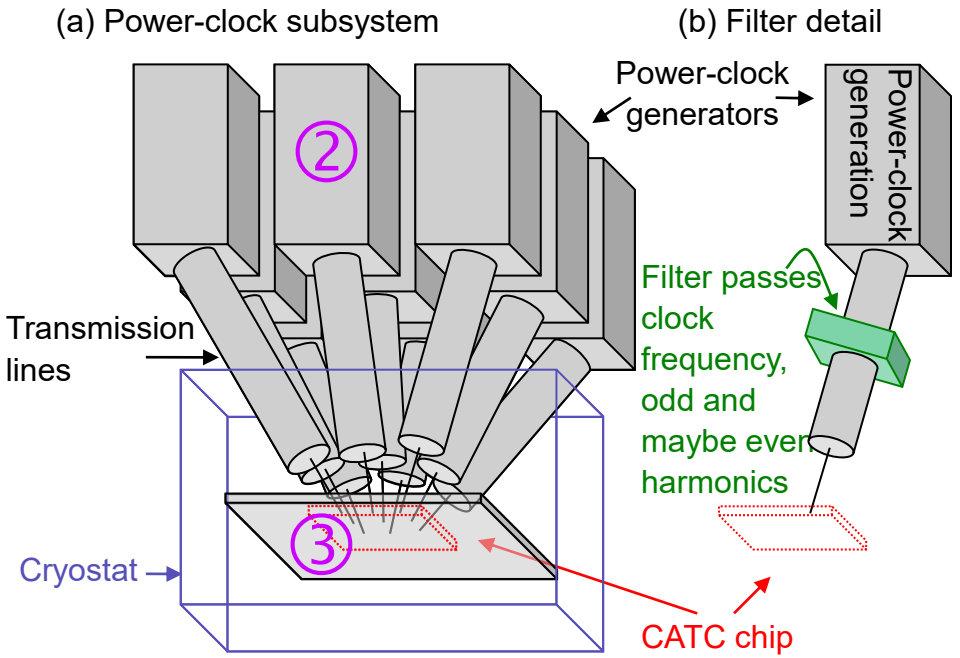
Q2LAL power-clocks

- Ramped power-clocks charge transistors gates
- No abrupt charging



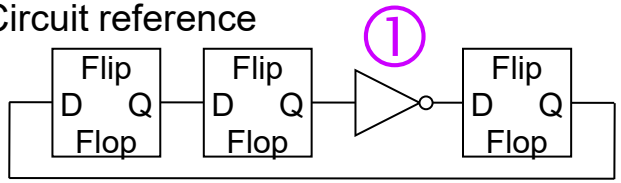
Q2LAL power train

- Power-clocks charge transistor gates) and then leave by reflection

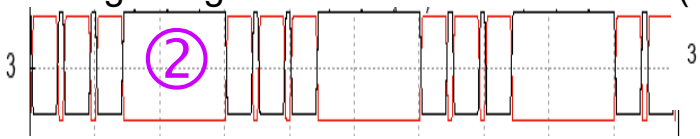


Even-load Adiabatic Logic Family Based on Cyber Security

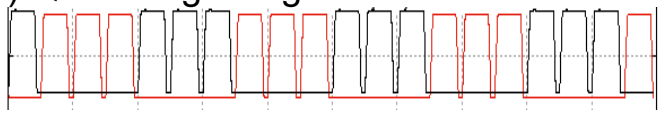
(a) Circuit reference



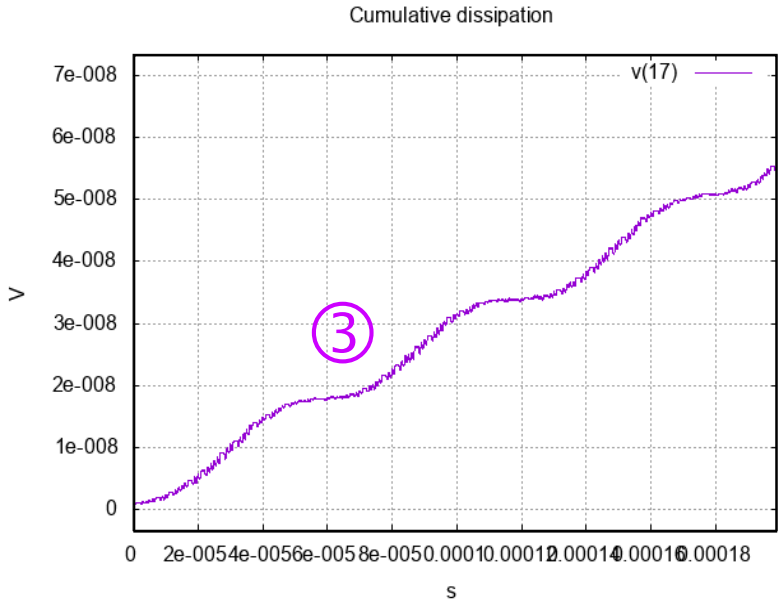
(b) S2LAL signaling



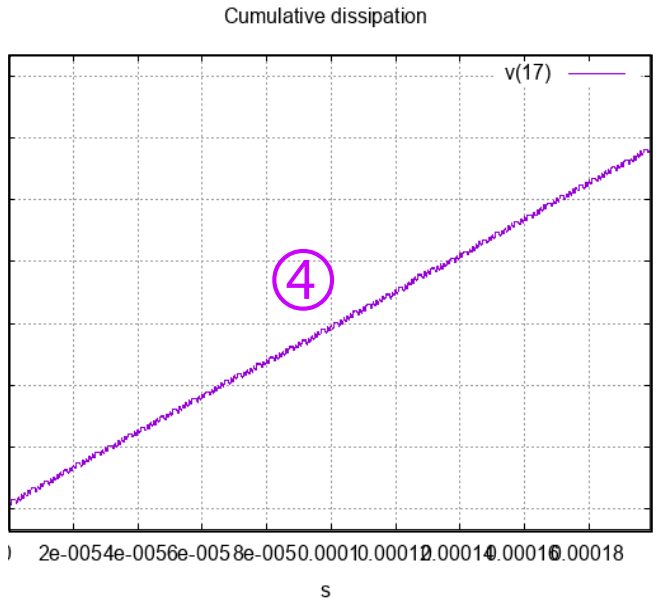
(d) Q2LAL signaling



(c) S2LAL + inverter

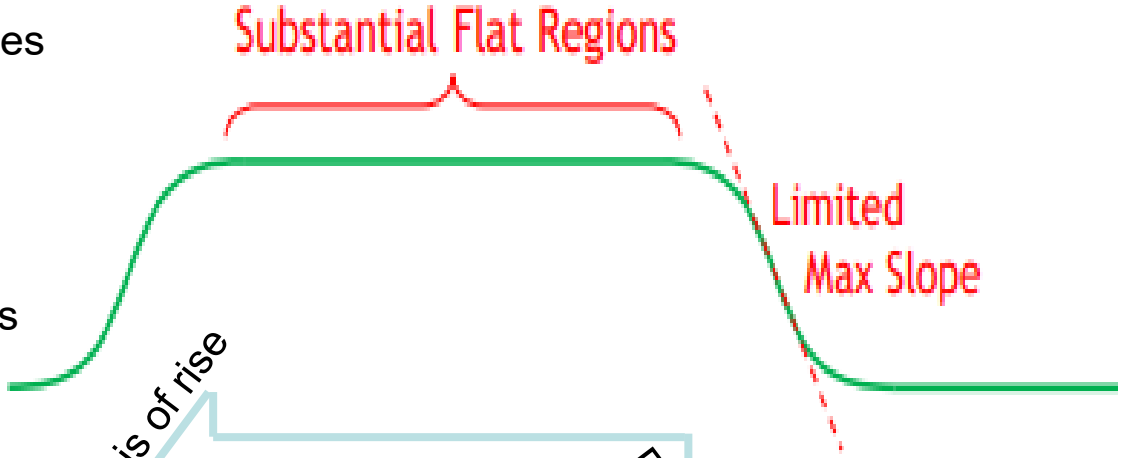


(e) Q2LAL + inverter



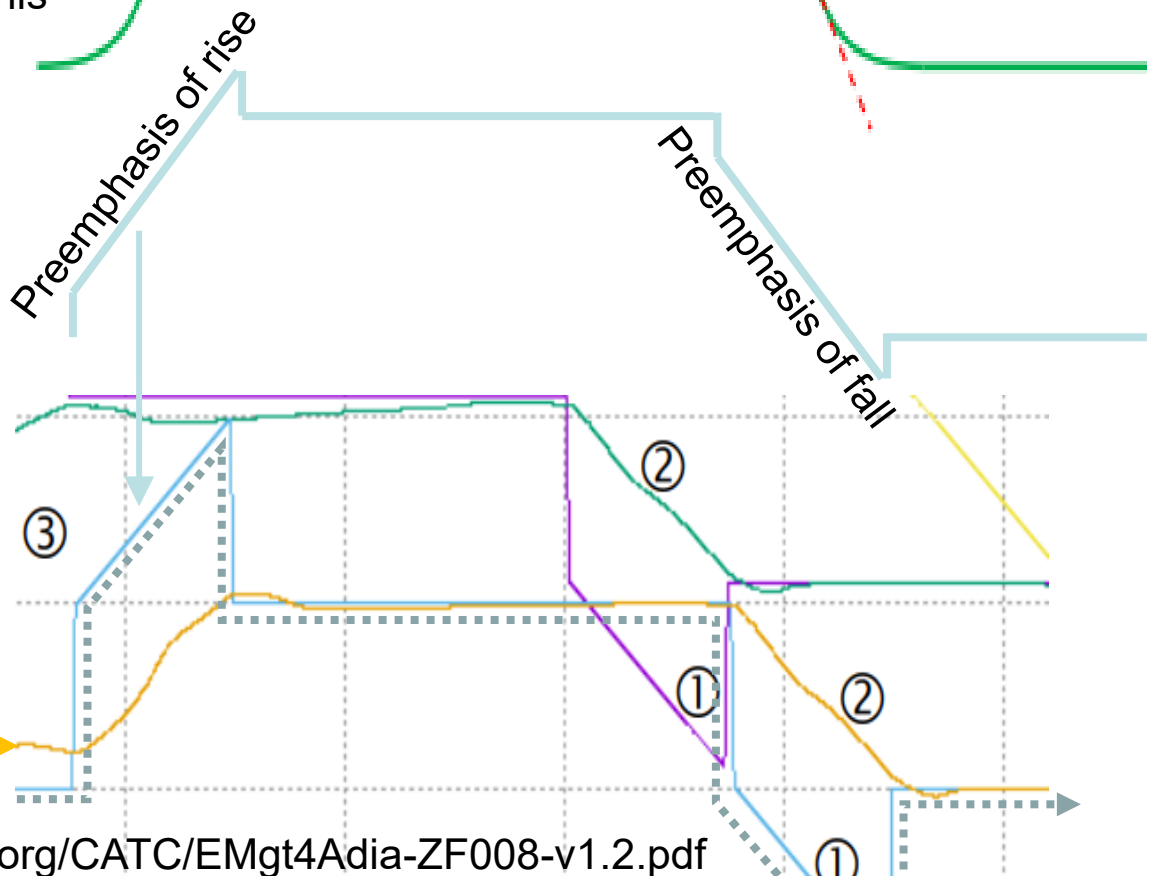
Data-enabled Clocks

Effect #1: Avoid current spikes



See Mike Frank's talk, this workshop

Effect #2: Preemphasis to reverse effect of distortion in signal transmission



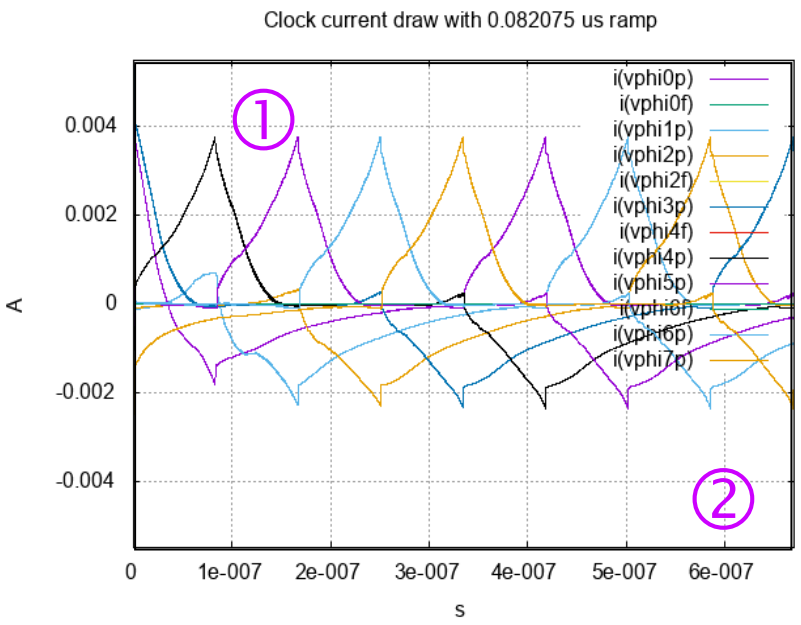
Simulation: Drive 500 loads in parallel through three feet of CATV transmission line

See: https://ar.zettaflops.org/CATC/EMgt4Adia-ZF008-v1.2.pdf

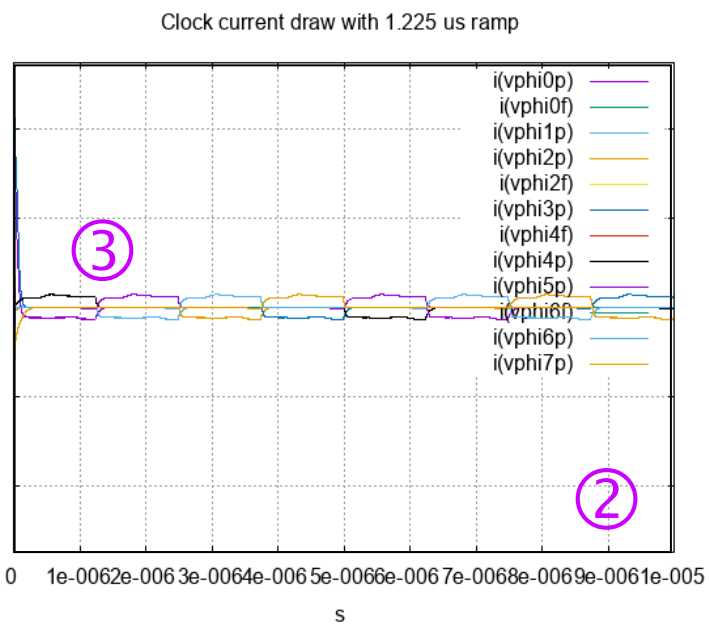
CMOS vs. CATC noise

- CMOS noise from delta functions with frequencies determined by devices
- CATC Noise from clock
- Below same vertical but 15× expanded horizontal scale

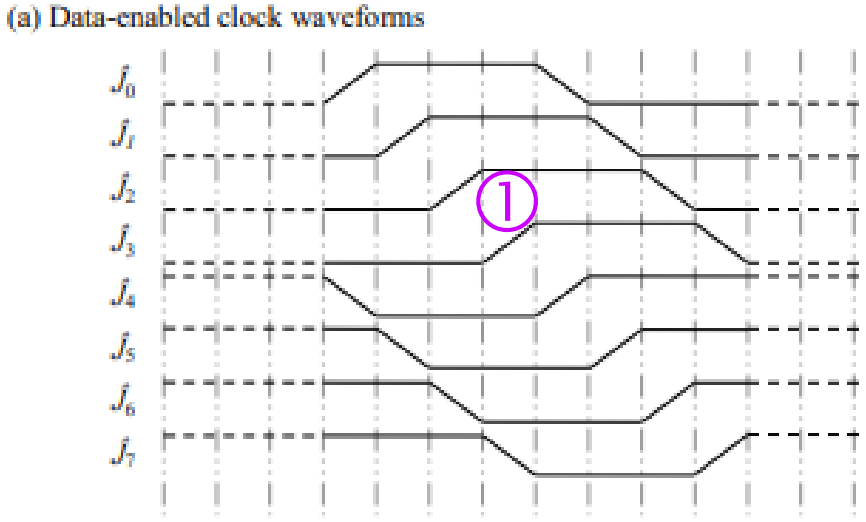
(a) Power-clock current at a reference clock period



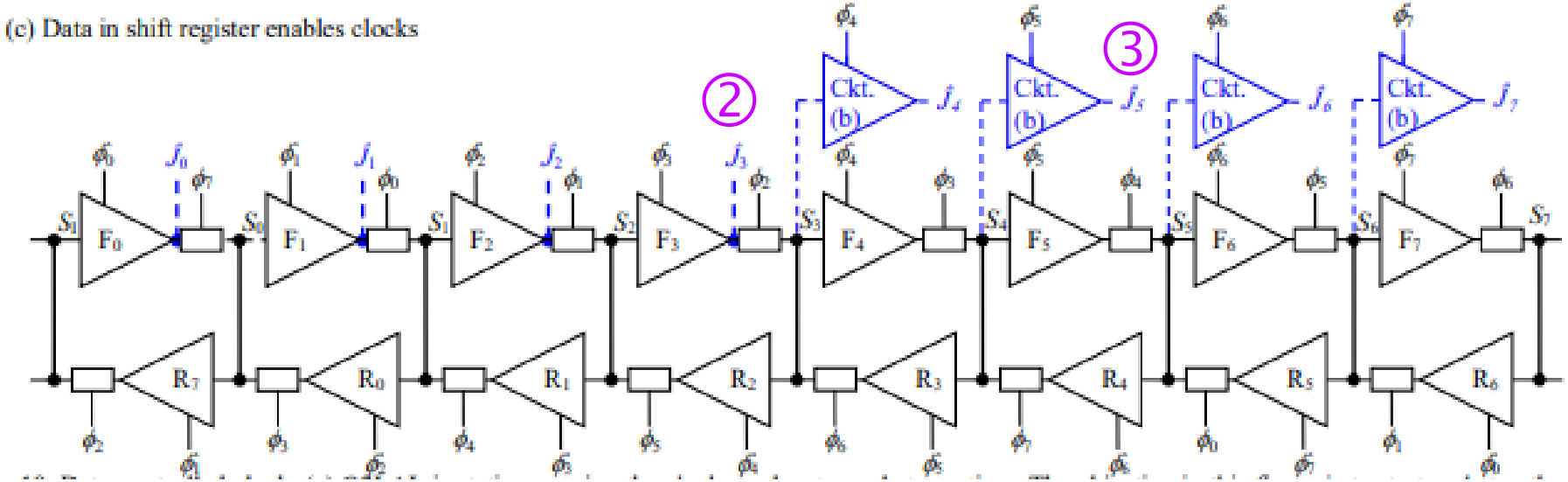
(b) Power-clock currant at 15× clock period



Data-enabled Clocks



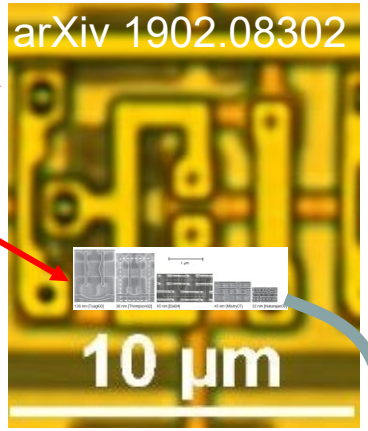
- A Q2LAL circuit that can gate a Q2LAL clock on and off
- Key to impleenting automata



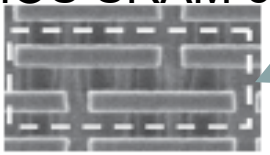
Single Flux Quantum (SFQ) and CATC Hybrid

Same scale;
JJs are larger
but very
energy efficient

JJ SRAM cell



CMOS SRAM cell



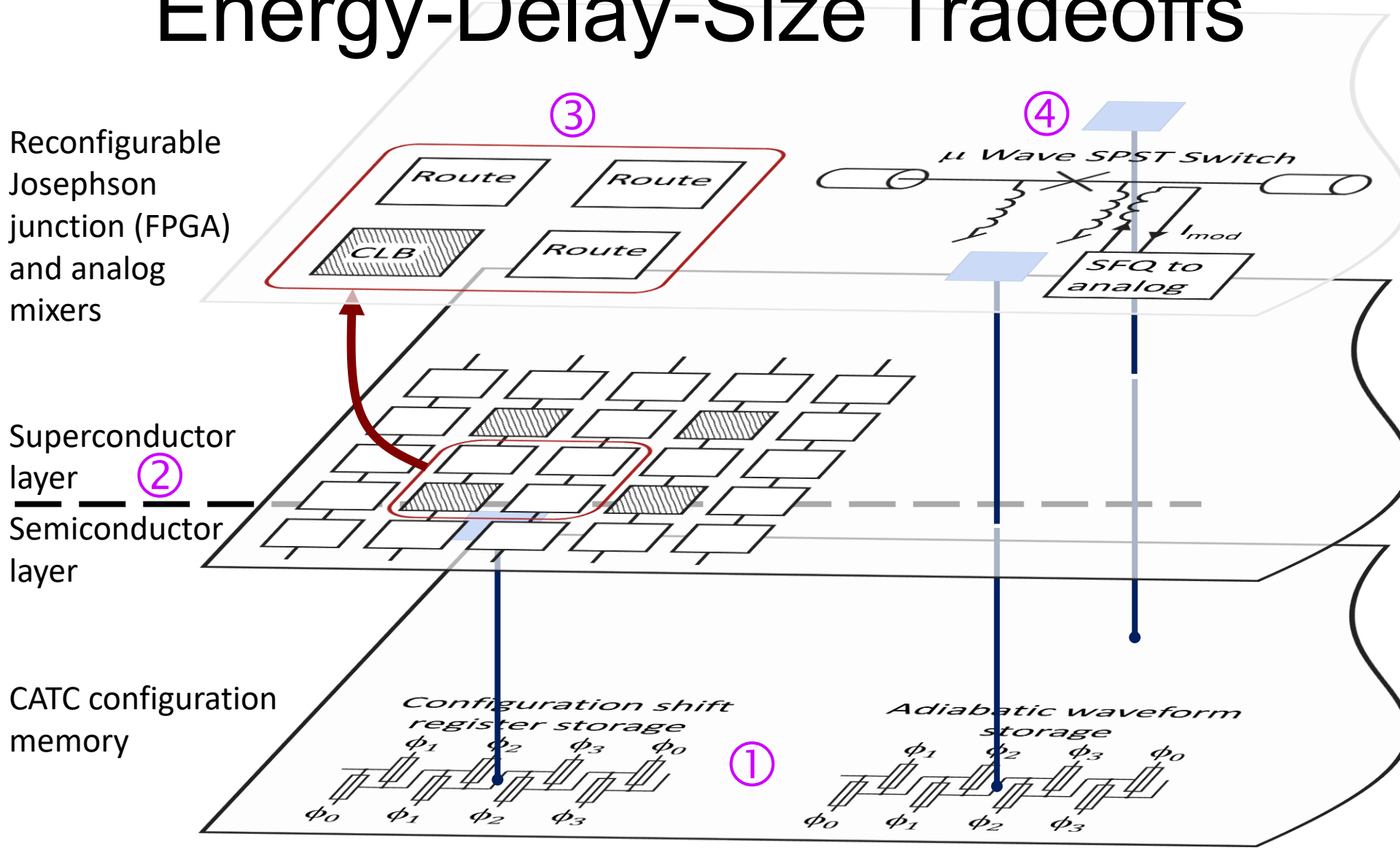
32 nm [Natarajan08]

1 μm

CMOS VLSI Design, Weste

- CATC vs. JJ/SFQ
  - ② CATC 1000× smaller
  - Same energy
  - CATC 1000× slower
- Why would you want JJs plus a lot of slow transistors? ③
  - Memory
  - Complex logic

Transistors/JJ Hybrid Exploits Energy-Delay-Size Tradeoffs



Conclusions

- Adiabatic circuits not new, but use case is new
  - Much of this talk could have been made 30 years ago
  - Use case, cryostat, low noise concern & Q2LAL new
- Benefits today:
  - Equivalent benefit to a 99.9%CV^2 reduction at room temperature by restructuring circuit and heat flow
  - Lower noise in terms of power, noise, and bandwidth
  - Invent (?) “perfectly adiabatic sequential logic”
- Future
  - Physical demo in quantum control use case
- For more information see https://zettaflops.org/isrds
  - These slides; full paper with simulation code, more