Cryogenic Adiabatic Transistor Circuits for Quantum Computer Control

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***Abstract*—Adiabatic and reversible computing have a previously unappreciated benefit that may make them important for quantum computing applications. While adiabatic and reversible methods did not catch on initially, they demonstrated ways to manage the location where waste energy is turned into heat. This work shows how to exploit this degree of freedom, explaining it with introduction of a new adiabatic logic family called Quiet 2-Level Adiabatic Logic (Q2LAL). In a hybrid room-temperature/cryogenic computing environment, such as a quantum computer, moving energy from the cryostat to room temperature before turning it into heat can save orders of magnitude in refrigeration energy and reduce electrical noise. The combination of the Q2LAL circuit and energy management strategy increases the range of applications suitable for adiabatic computing.**

Keywords—adiabatic computing; reversible computing; quantum computer; CMOS; cryo CMOS; Quiet 2-Level Adiabatic Logic; Q2LAL

I. Introduction

Adiabatic and reversible circuits have been a theoretical possibility for improving the energy efficiency of classical computation for a half century. In the last few years quantum computing has attracted interest due to the possibility it may challenge the microprocessor as a commercially interesting use case. This work shows how to adapt adiabatic and reversible principles for the classical control portion of a quantum computer.

The adaptations lead to a novel "adiabatic power train," i. e. the stages that power goes through between its production and the creation of a useful result.

II. Quantum Use Case

A quantum computer will require both classical and quantum components—and scaling up a quantum computer is now believed to require some classical electronics to be collocated with the qubits in the cryogenic environment, albeit only for qubit types that require cryogenic operation.

Fig. 1a shows the primitive operation of preparing a |0> state. The first step is to take qubit in an arbitrary state and measure it. If the result is a 0, the process completes but if it is a 1, the qubit is flipped from |1> to |0>. Fig. 1b shows how multiple instances of this function can be performed in parallel using a single microwave wave form generated at room temperature. A classical flip flop controls a microwave switch collocated with a qubit.

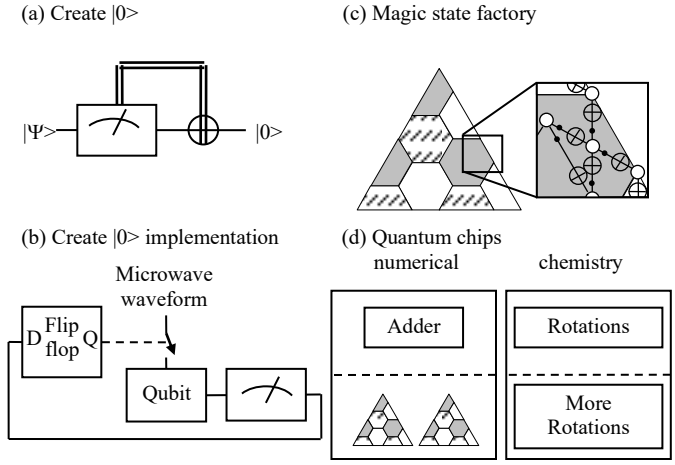


Fig. 1. (a) Circuit for creating |0> and (b) classical-quantum implementation with integrated microwave blocking. (c) Magic state factory [1] and (d) reconfiguration of a quantum chip for numerical and chemistry problems.

Fig. 1c shows a structure for preparing magic states [1], which is a schematic like the space-time layout of a classical arithmetic unit. Magic state preparation includes many preparations of |0> along with other operations. The magic state factories can be embedded in the quantum chip shown in Fig. 1d. The quantum chip in turn could be reconfigured to have adders for algebraic problems and rotation gates for chemistry simulations. Quantum adders use magic states as their main resource.

These use cases all require cryogenic digital sequential logic or automata. To scale these use cases requires high energy efficiency to avoid overloading refrigeration systems.

III. The Historical Adiabatic Opportunity

Fig. 2 shows a well-known graph of Spice simulations of energy per operation for a CMOS circuit versus an adiabatic circuit built from the same transistors. The horizontal curves are for CMOS, which are level at energy $\frac{1}{2}CV^2$ irrespective of the clock period on the horizontal axis. However, the 2-level adiabatic logic (2LAL) family [2] shows a linear decrease in energy per operation as the clock period increases, reaching a 10^3 reduction at a 10^3 longer clock period. The curves should follow the purple arrow further, but neither Spice nor transistors have been "debugged" for cryogenic adiabatic operation.

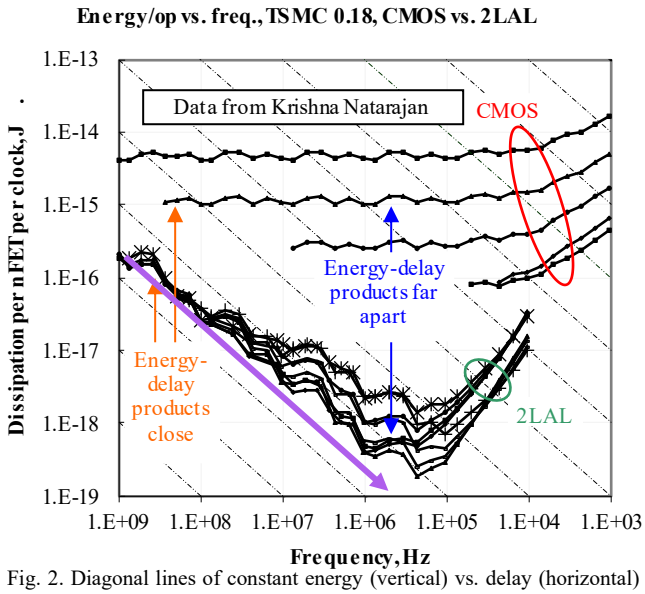


Fig. 2. Diagonal lines of constant energy (vertical) vs. delay (horizontal) product become straight lines sloping downward at –45° on a log-log scale (parallel to the purple arrow). CMOS (orange) and adiabatic circuits (green) are fairly close in energy-delay product at high speeds. However, 2LAL and other adiabatic circuits maintain the energy-delay product along the purple line, giving adiabatic circuits an advantage (blue).

While Fig. 2 looks compelling, the graphs show the power consumption of an adiabatic chip measured at its terminals. This is like rating an automobile by the power delivered to the tires. It is also important to assess the efficiency by which the automobile's transmission matches engine speed to tire speed. It will turn out that the most effective adiabatic power train is different when supplying power to a cryogenic adiabatic chip than one at room temperature.

The power-clock waveform generator for a room-temperature adiabatic chip must source a waveform during one part of the cycle and then reabsorb the energy in that waveform during another part of the cycle. To match the energy efficiency of the chip shown in Fig. 2 would require a power supply that can recycle energy with 99.9% efficiency. This efficiency requirement leads to the idea of resonant power supplies, which have not been perfected to date.

IV. The Adiabatic Power Train

The adiabatic power train in Fig. 3 generates the power-clock waveforms at room temperature and sends them down transmission lines to the cryogenic adiabatic transistor circuit (CATC) shown in red.

The voltage on the waveform will enter the chip and follow the myriad internal wires and end up on the gates of transistors, which are capacitors. While there are resistive losses as the waveform passes through turned-on transmission gates, these losses decline as the clock period increases, giving the transmission line a capacitive termination.

An improperly terminated transmission line creates a reflected wave in the opposite direction, or back to room temperature. Since the termination is reactive, the reflection will be distorted but if the capacitance is pure, the reflected

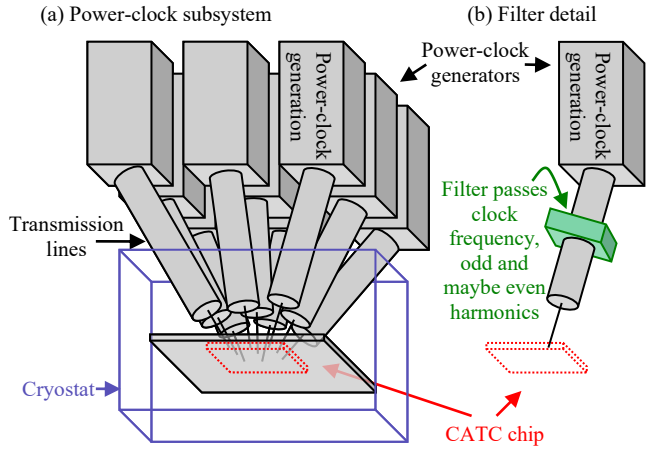


Fig. 3. Power-clock subsystem. (a) Overview comprising signal generators, transmission lines to cold space, and CATC chip. (b) Filter on transmission line.

wave will have as much energy as the incident wave. The result shown in Fig. 2 is that the heat dissipated by the CATC chip is proportional to the RC time constant divided by the clock period, dropping linearly as shown by the purple arrow. The remaining energy flows back up the transmission line to room temperature, where the cost of energy is 1,000× lower than at (for example) 4 K.

Thus, the adiabatic power train gives good results even in the absence of energy recycling. Since the cost of energy is lower, moving waste energy to room temperature before turning it into heat saves 1,000× in wall plug energy.

$\frac{1}{2}CV^2$ is the same for CMOS and an adiabatic circuit, but toward the tip of the purple arrow in Fig. 2, 99.9% of the incident energy would be reflected up the transmission line while 0.1% would turn into heat and removed by the cryo refrigerator with 1,000× overhead. Thus, CMOS would draw $500CV^2$ from the wall plug for each signal transition versus CV^2 for the adiabatic circuit.

V. Load Variance

Most logic circuits, adiabatic and otherwise, use a different amount of energy when processing a 1 compared to a 0. For example, 1s may be signaled by a voltage transition while 0s remain at a DC level. If an adiabatic circuit with this property is applied to Fig. 3, the capacitive loading on the transmission line will vary depending on data in the circuit, distorting the AC waveform into an improper shape for energy recovery and creating excess heat.

However, adiabatic circuits have been devised for computer security purposes that use the same amount of energy irrespective of data, such as EE-SPFAL [3]. This work involved applying a similar technique to the Static 2LAL (S2LAL) circuit family [4], yielding Quiet 2LAL (Q2LAL) [5] which has the same electrical properties when processing 0s and 1s.

Fig. 4a shows a test circuit where the flip flops go from all zeros to all ones, as shown by one of the data waveforms in

Fig. 4b. The differing numbers of transitions per clock cycle led to the wavy cumulative dissipation curve in Fig. 4c, reflecting uneven loading. However, a Q2LAL circuit has the same number of transitions per unit time as shown in Fig. 4d and constant dissipation as illustrated in Fig. 4e.

To create the correct wave shape, the clock-power generators in Fig. 2 can apply a predistortion that would be cancelled by the distortion due to the improper termination at the chip. With a constant load, this predistortion does not change over time and the system works as expected.

VI. Noise

CMOS produces a lot more electrical noise than Q2LAL, making CMOS more likely to decohere qubits.

CMOS switches via a transistor turning on or off abruptly. The result is a step function in voltage or a delta function in power supply current. These wave forms will have time constants in the handful of picoseconds (for nodes with short wires) and produce a white noise spectrum up 100 GHz or more. This white noise covers qubit control frequencies, which are in the single-digit gigahertz. Thus, CMOS switching noise must be considered as a source of qubit decoherence.

However, Q2LAL's noise originates with the power-clock signals—but the engineer has a lot of control over these signals. Since an adiabatic power-clock waveform is not a sine wave, it must include harmonics up to about 10× the base frequency to maintain the required shape. The purple arrow in Fig. 1 represents harmonics of 10 MHz–10 GHz, most of which is below qubit control frequencies.

Fig. 5 shows explicit simulations of noise, specifically plots of current drawn from the AC power supply (as measured at the chip). Fig. 5a shows these currents for an arbitrary base frequency while Fig. 5b shows the current on the same vertical scale at a 15× longer clock period but with a 15× larger horizontal scale. In other words, Figs. 3a and b are logically the same but there is a 15× time expansion between the two.

The reader will see that the noise amplitude drops but the number of horizontal features is about the same. Since the time scale is longer in Fig. 5b, the frequencies drop. A more extensive analysis, beyond the scope of this extended abstract, shows the reduction in noise amplitude and frequency spectrum is a general and ongoing property of this circuit class. The ultimate wave shape in Fig. 5b can also be engineered to trade noise spectrum for energy efficiency within some bounds.

VII. Other Issues

Due to length limitations in this extended abstract, I will simply state that this work also included analysis of other issues that are in the video of the conference talk and may appear in an expanded version of this document:

The fact that the load and hence applied waveform does not change allows very tight filtering to be placed on the transmission line, as shown in Fig. 3b, preventing noise from the room-temperature environment from entering the cryostat via the clock power lines.

There was also work showing how to extend the concept of adiabatic logic to adiabatic sequential logic and automata. This included the idea of adiabatic subsystems on the same chip

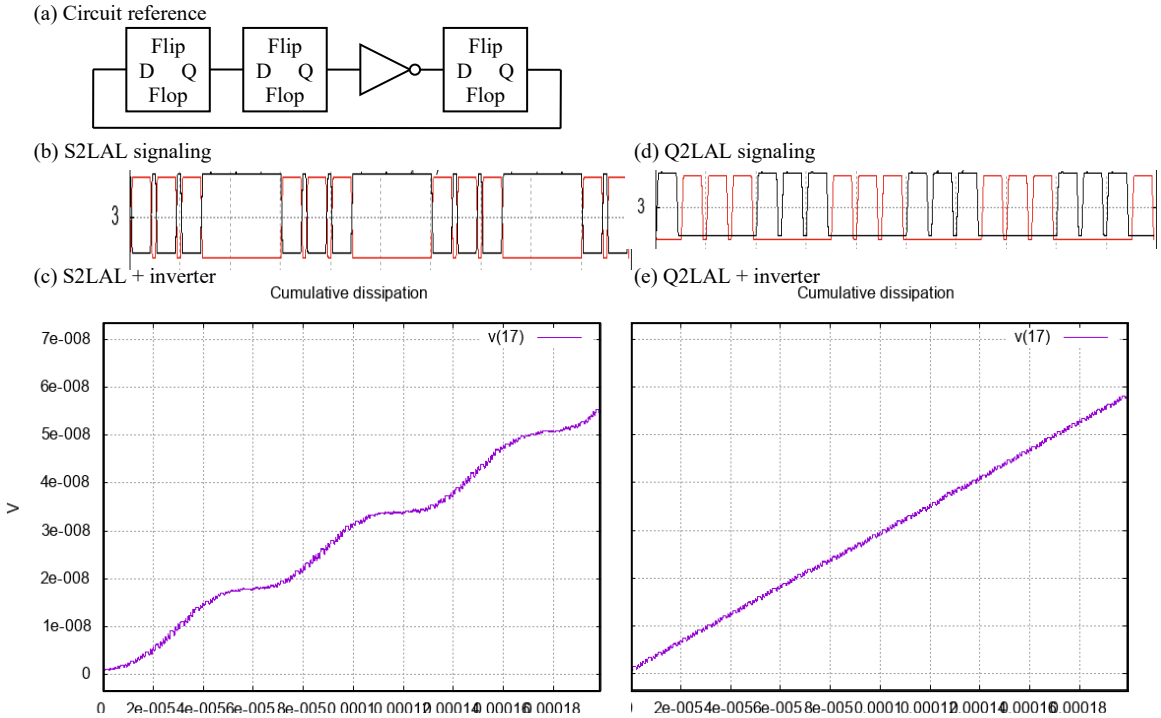


Fig. 4. (a) Circuit reference, generating repeating sequence 000 100 110 111 011 001. (b) S2LAL output $\hat{Q}$ and $\check{Q}$ (red and black) showing one bit position in the circuit (c) S2LAL cumulative dissipation, showing variance as the number of 1s changes. (d) Q2LAL signaling, where either $\hat{Q}$ or $-\hat{Q}$ is a 1 on each clock (e) Q2LAL dissipation, where the total number of 0s and 1s does not change and so the dissipation is constant.

running at different clock rates. There is a circuit whereby subsystems at different clock rates can exchange data. There are also circuits allowing subsystems to be arranged in a hierarchy where a subsystem's clock could be turned on or off by subsystems higher up the hierarchy. The result can be used to create sequential logic or automata for the behavior in Fig. 1, such as creating |0> and magic states.

Many quantum computers are implemented today as a room-temperature Field Programmable Gate Array (FPGA). A hybrid of Q2LAL and Single-Flux Quantum (SFQ) circuits could yield a work-alike system yet where the FPGA could be in the cryogenic environment. This would reduce the amount of wiring in and out of the cryostat—and the heat backflow and latency it brings. The hybrid FPGA is mentioned in the video of the conference talk.

VIII. Conclusions

Classical logic families are an abstraction that required their creators to minimize interactions with the environment. Quantum computers offer higher performance but go to the other extreme of requiring an environment with specific properties, such as cryogenic operating temperatures, the absence of electromagnetic noise, phonons, impure materials, and so forth.

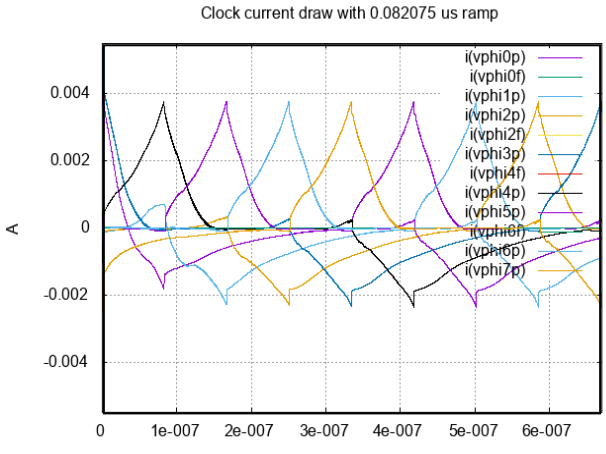
This work backtracked on some cherished principles of computer engineering by designing a logic family that goes out of its way to exploit its environment, such as a temperature difference, and gives the engineer the ability to tune the computer's internal structure to meet application requirements, such a minimizing noise.

This work involved developing the Q2LAL logic family, whose reference has not been officially published at this time. However, unpublished ref. [5] includes the circuit diagrams for Q2LAL and includes an appendix with ngspice code containing both S2LAL and Q2LAL circuits. Running the code with appropriate flags will compare S2LAL and Q2LAL, creating the plots in Fig. 4. Running the ngspice code in the last slide of ref. [6] will create the noise plots in Fig. 5.

Acknowledgment

Michael P. Frank has made many contributions to reversible computing over the years. Mike developed S2LAL [4], from which Q2LAL is derived. Mike also championed a framework and notation that applied to at least the families SCRL, 2LAL [1], and S2LAL—and which I used both in developing Q2LAL, so there are now four uses of the notation and framework.

(a) Power-clock current at a reference clock period



(b) Power-clock currant at 15× clock period

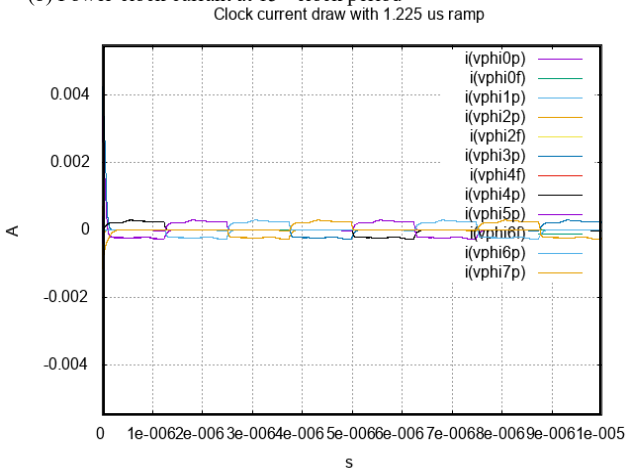


Fig. 5. Q2LAL power supply noise. (a)-(d) Ngspice simulation of circuit in Fig 6c, showing the 8 power-clocks a an arbitrary clock period and 1.5, 15, and 150× the clock period. The length of the simulation increases at the same rate as the clock period, so the data is the same. As speed decreases, clock current becomes a constant charge/discharge current that switches from one clock phase to another.

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