

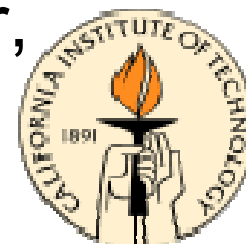
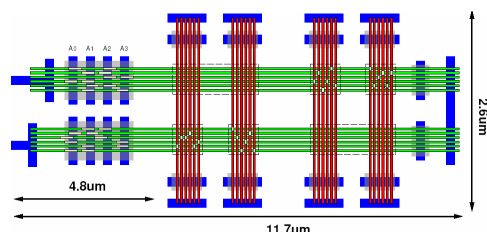
Nanowire-Based Computing Systems

André DeHon

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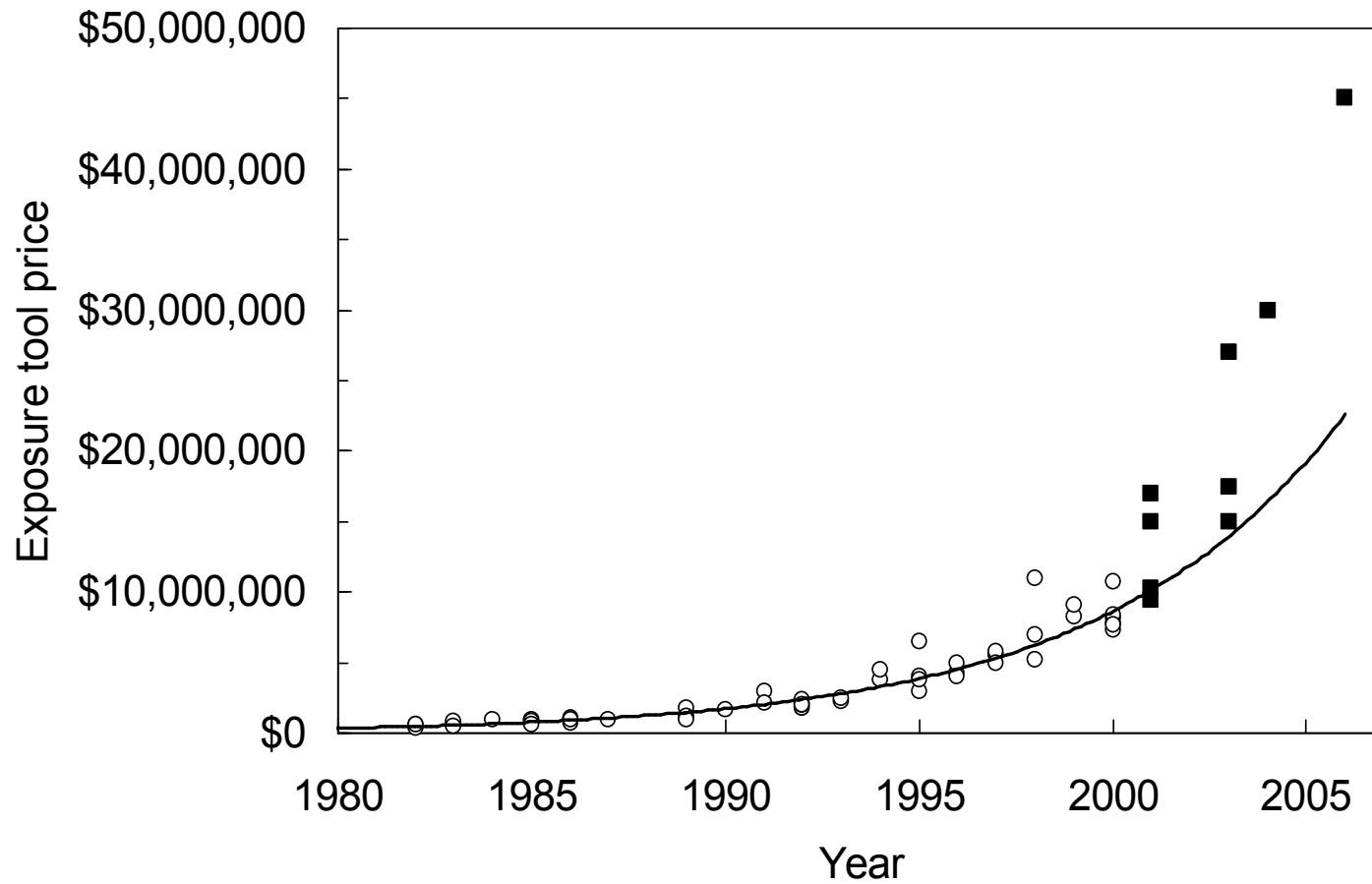
In collaboration with

Helia Naeimi, Michael Wilson, Charles Lieber,
Patrick Lincoln, and John Savage



CHIP FABRICATION COSTS

Moore's Second Law ("Rock's Law")



Kahng (2001)

Question

- Can we build interesting computing systems using bottom-up, nanoscale building blocks?
 - *E.g.* nanowires
 - without using lithographic patterning for our smallest feature sizes?

Focus Challenge

- How build programmable logic from nanowires and molecular-scale switches?
 - With regular self-assembly
 - Only have statistical differentiation
 - With high defect rates

Today's Talk

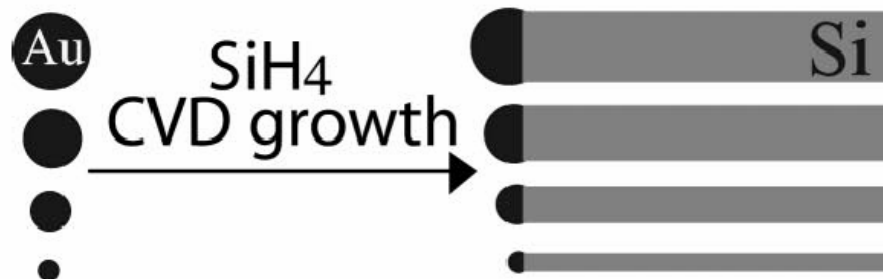
Bottom up tour: from Si atoms to Computing

- Nanowire Building Blocks
 - growth
 - devices
 - assembly
 - differentiation
 - coding
- Logic: nanoPLAs
- Analysis

Building Blocks

Semiconducting Nanowires

- Few nm's in diameter (*e.g.* 3nm)
 - Diameter controlled by seed catalyst
- Can be microns long
- Control electrical properties via doping
 - Materials in environment during growth
 - Control thresholds for conduction



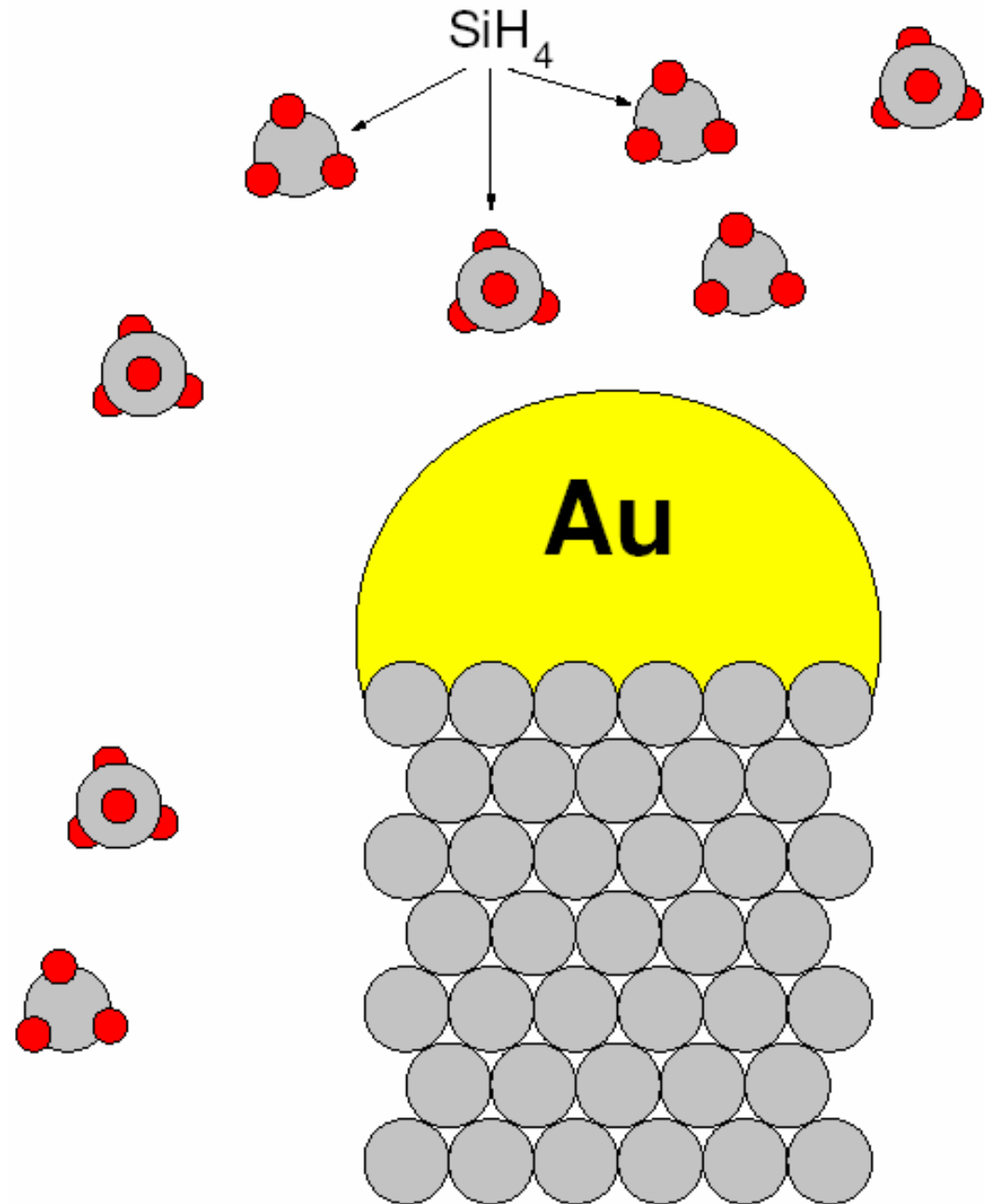
From:

Cui...Lieber

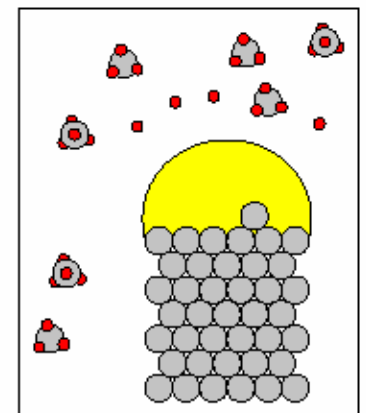
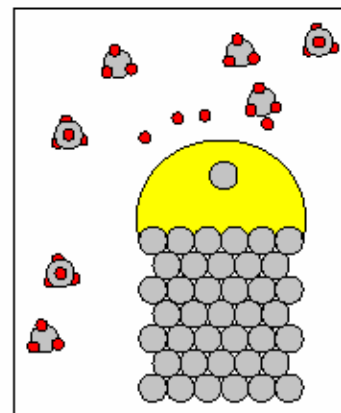
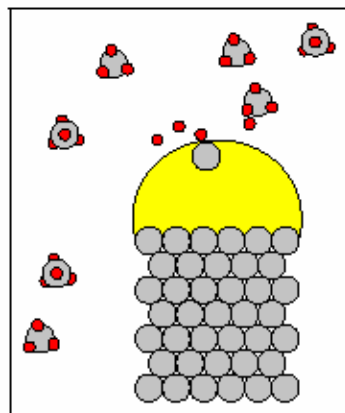
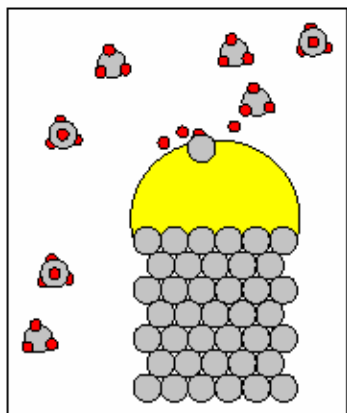
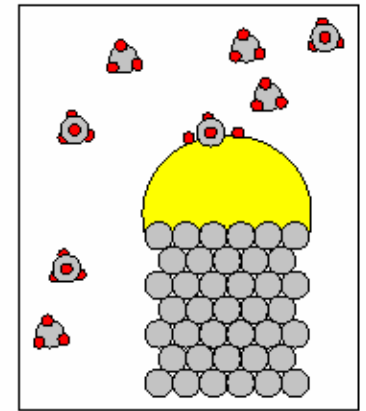
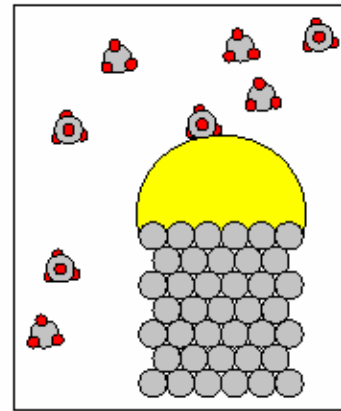
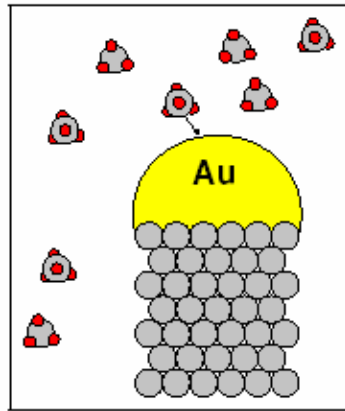
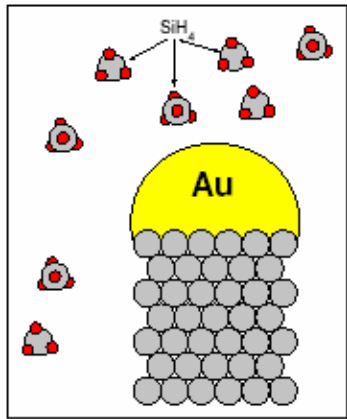
APL v78n15p2214

SiNW Growth

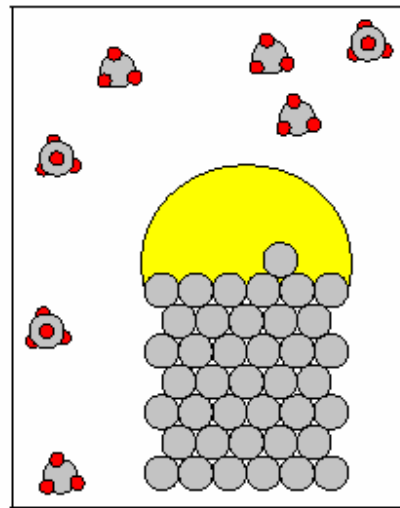
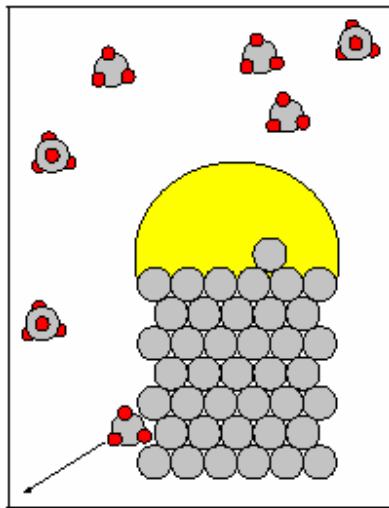
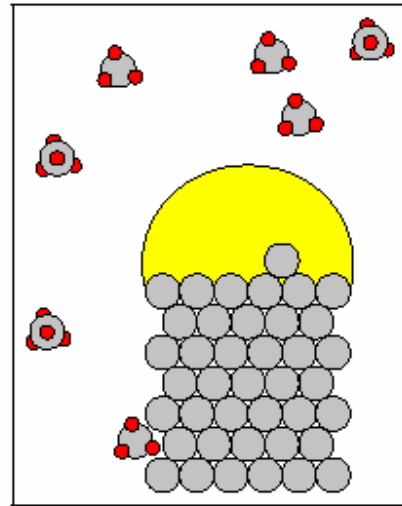
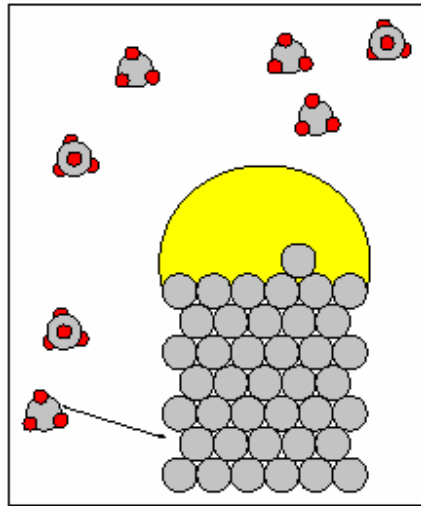
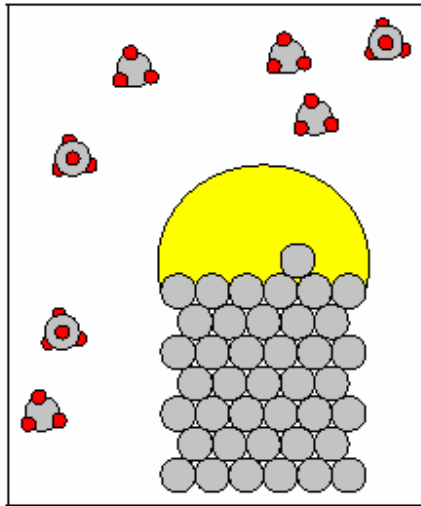
- Self-same crystal structure constrains growth
- Catalyst defines/constrains structure



SiNW Growth

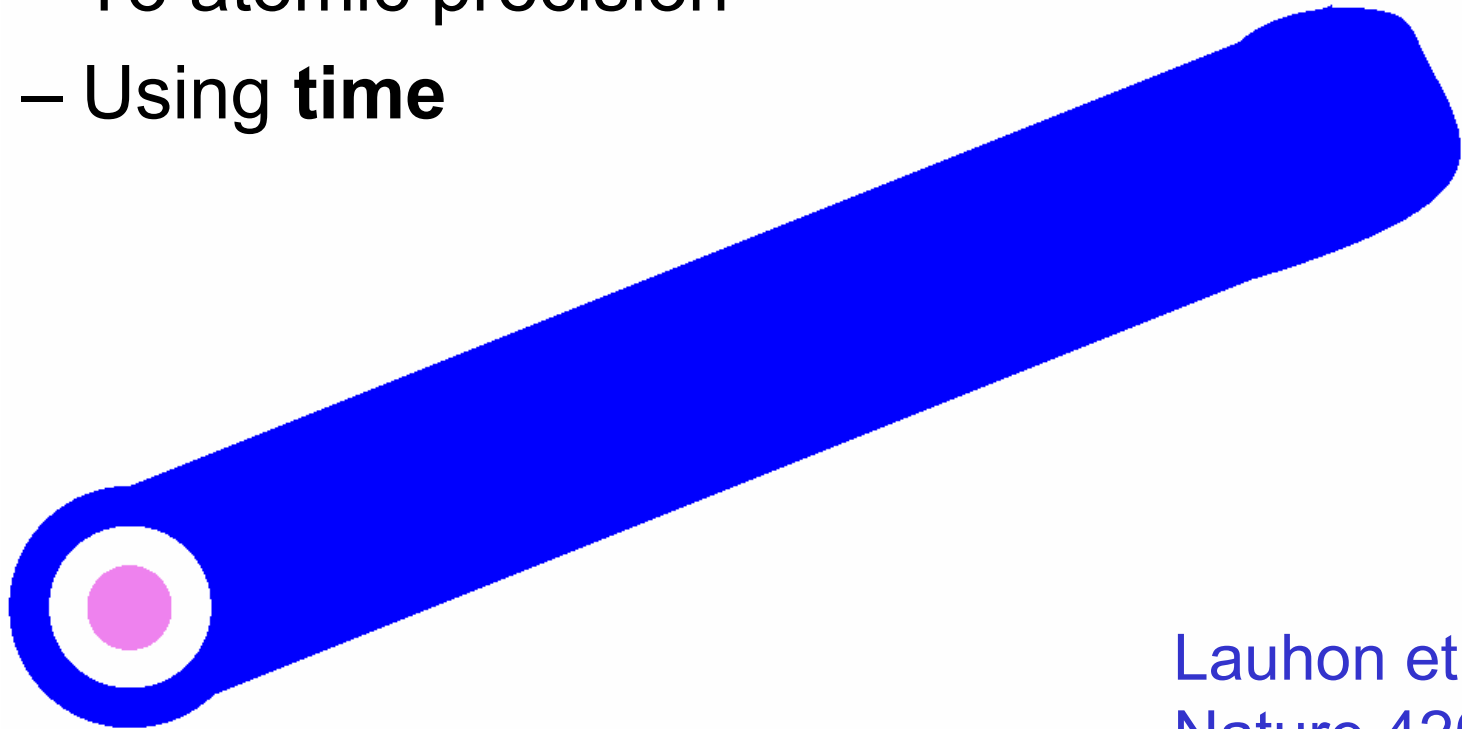


SiNW Growth



Radial Modulation Doping

- Can also control doping profile radially
 - To atomic precision
 - Using **time**

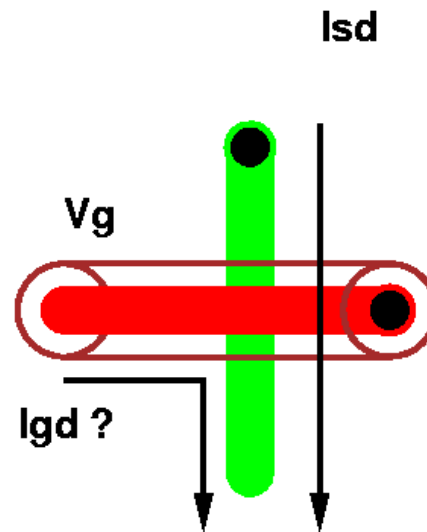
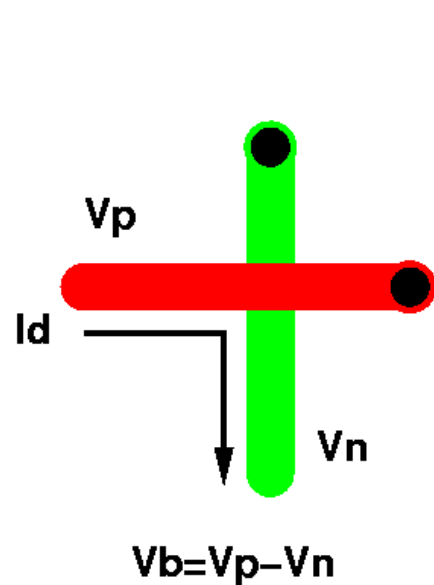


Lauhon et. al.
Nature 420 p57

Devices

Doped nanowires give:

Diode and FET Junctions



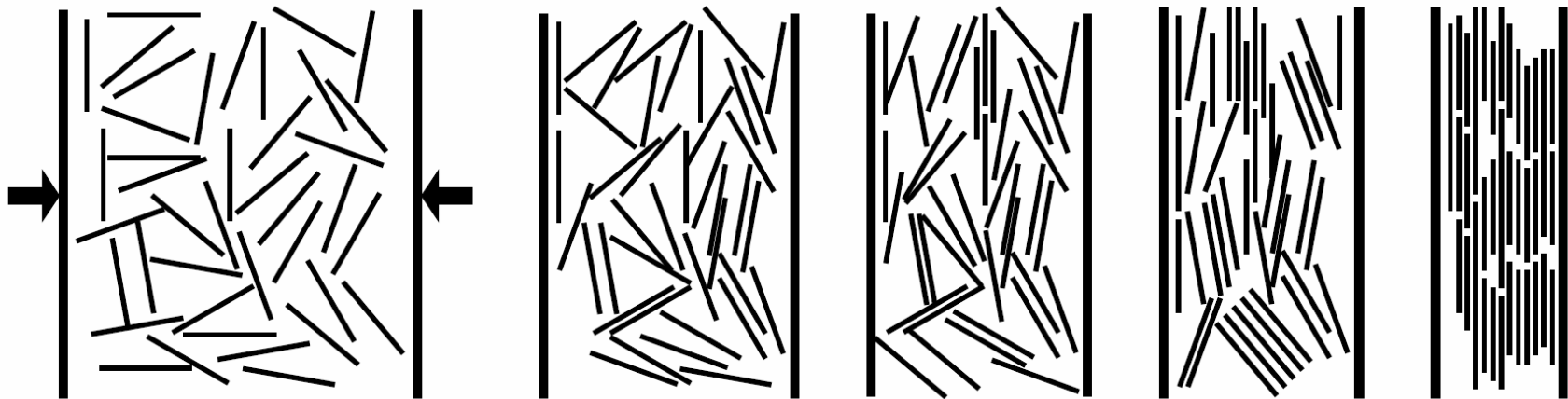
Cui...Lieber
Science 291 p851

FEC 2005 -- DeHon

Huang...Lieber
Science 294 p1313

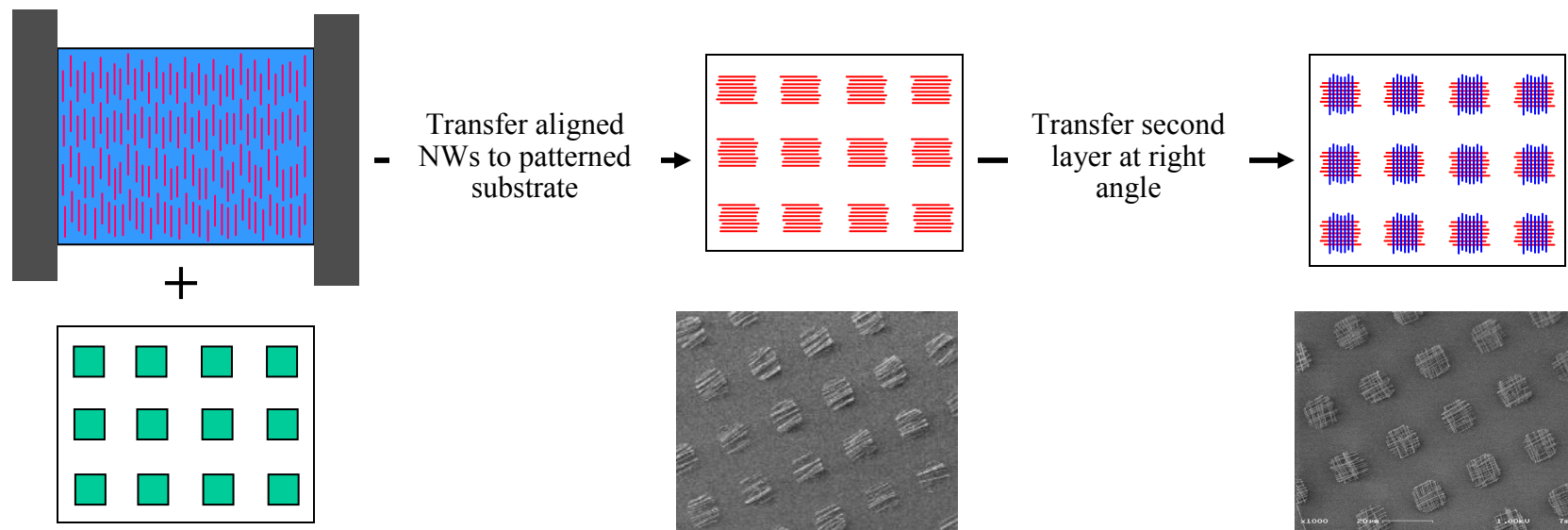
Langmuir-Blodgett (LB) transfer

- Align Nanowires



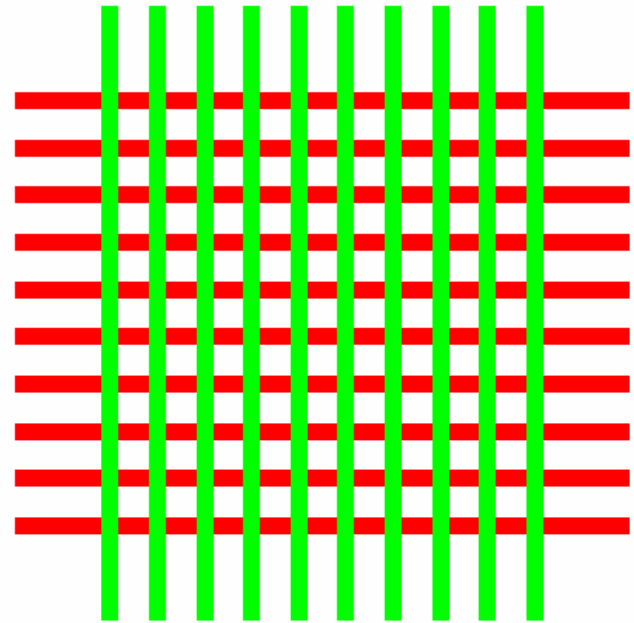
Langmuir-Blodgett (LB) transfer

- Can transfer tight-packed, aligned SiNWs onto surface
 - Maybe grow sacrificial outer radius, close pack, and etch away to control spacing



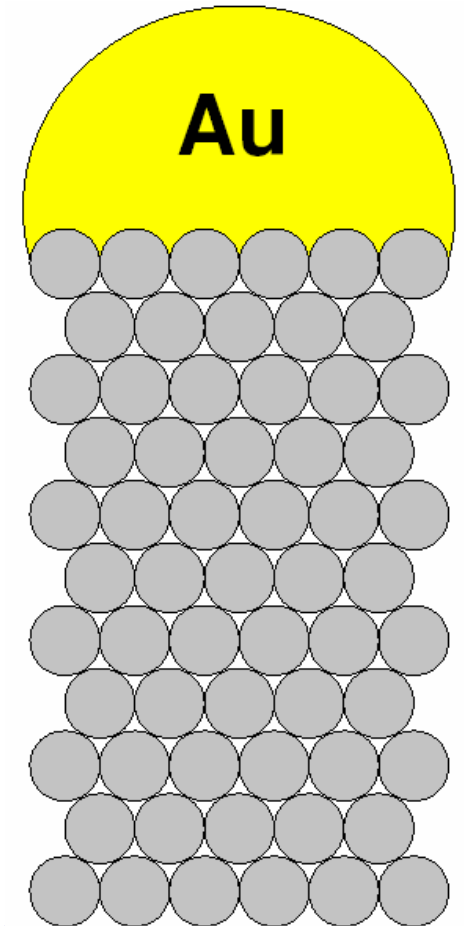
Homogeneous Crossbar

- Gives us homogeneous NW crossbar
 - Undifferentiated wires
 - All do the same thing
- Can we build arbitrary logic starting with regular assembly?



Control NW Dopant

- Can define a dopant profile along the length of a wire
 - Control lengths by **timed** growth
 - Change impurities present in the environment as a function of time



Gudiksen et al.
Nature 415 p617

Björk et al.
Nanoletters 2 p87

Control NW Dopant

- Can define a dopant profile along the length of a wire
 - Control lengths by **timed** growth
 - Change impurities present in the environment as a function of time
- Get a SiNW banded with differentiated conduction/gate-able regions



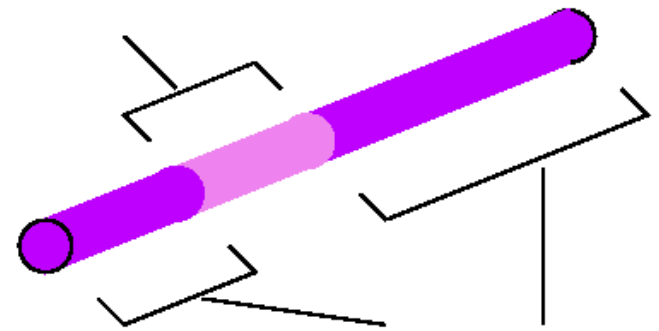
Gudskien et. al.
Nature 415 p617

Björk et. al.
Nanoletters 2 p87

Enables: Differentiated Wires

- Can engineer wires
 - Portions of wire always conduct
 - Portions controllable

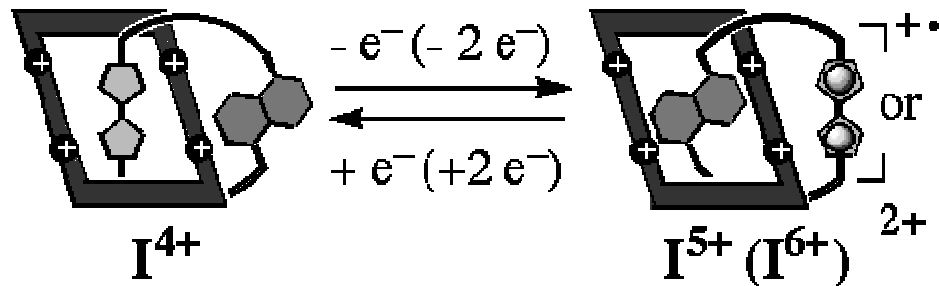
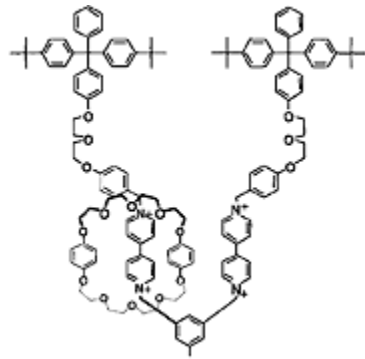
Conduct only
with field $< 1\text{ V}$



Conduct any field $< 5\text{V}$

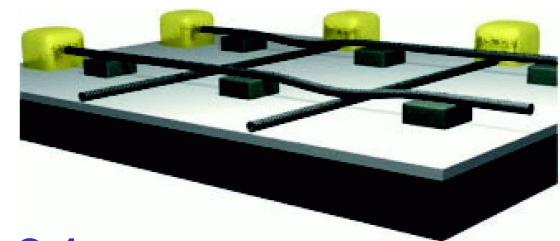
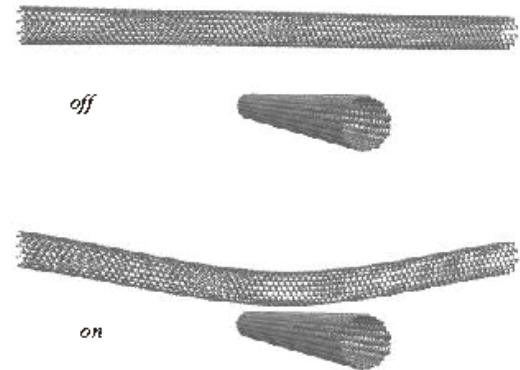
Switches / Memories

Molecular Switches



Collier et al.
Science 289 p1172

Electrostatic Switches

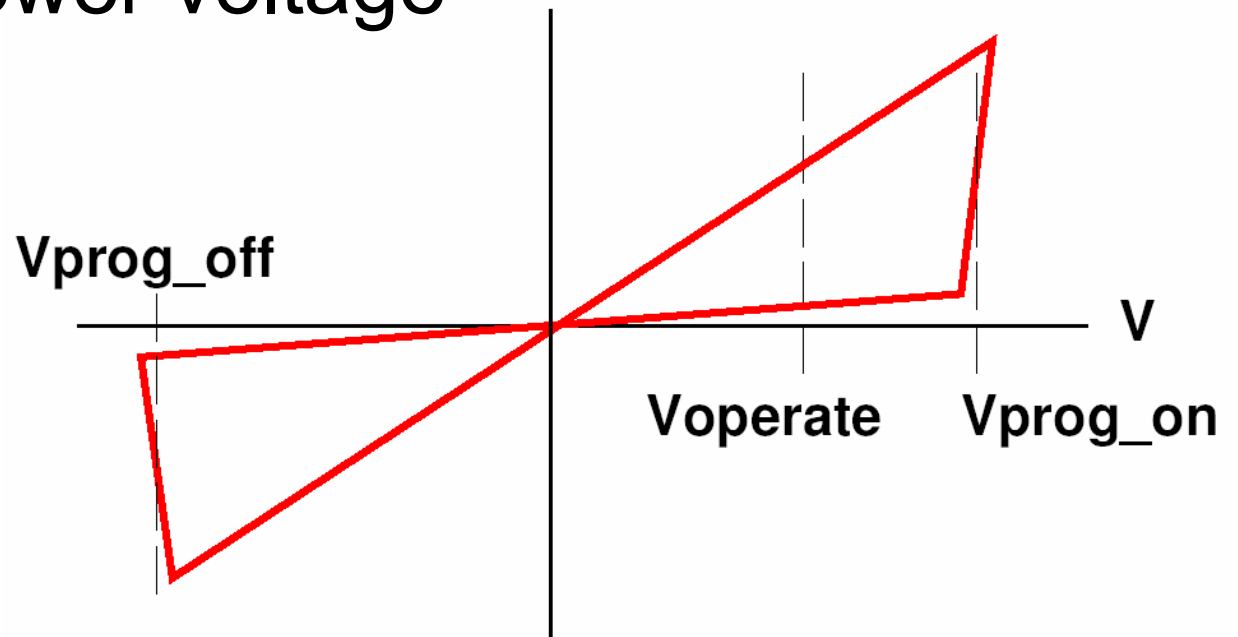


Ruekes et al.
Science 289 p04

Common Switchpoint Properties

- Fit in space of NW crossing
- Hysteretic I-V curves
- Set/reset with large differential voltage across crosspoint
- Operate at lower voltage ^I

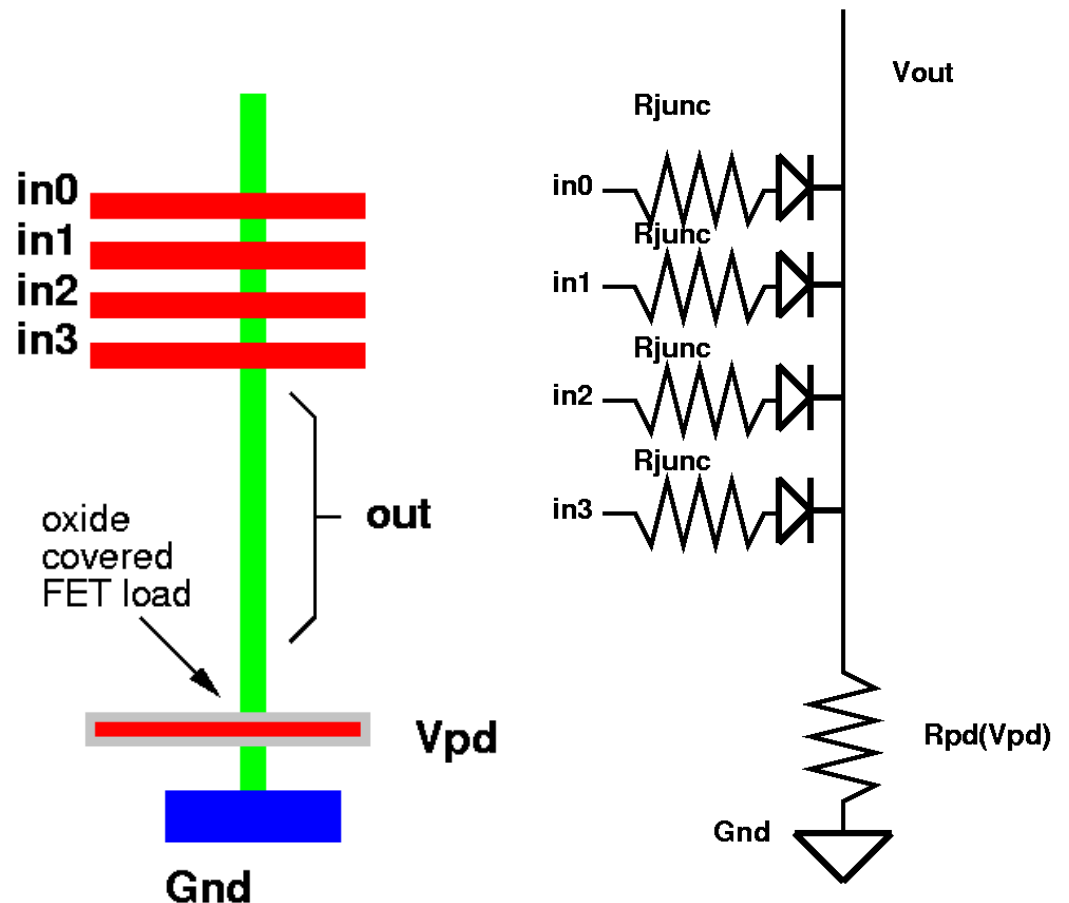
- Molecular Switch
- Filamental Metal
- Floating Gate
- Ferro-electric
- Electro-mechanical
- δ -doped



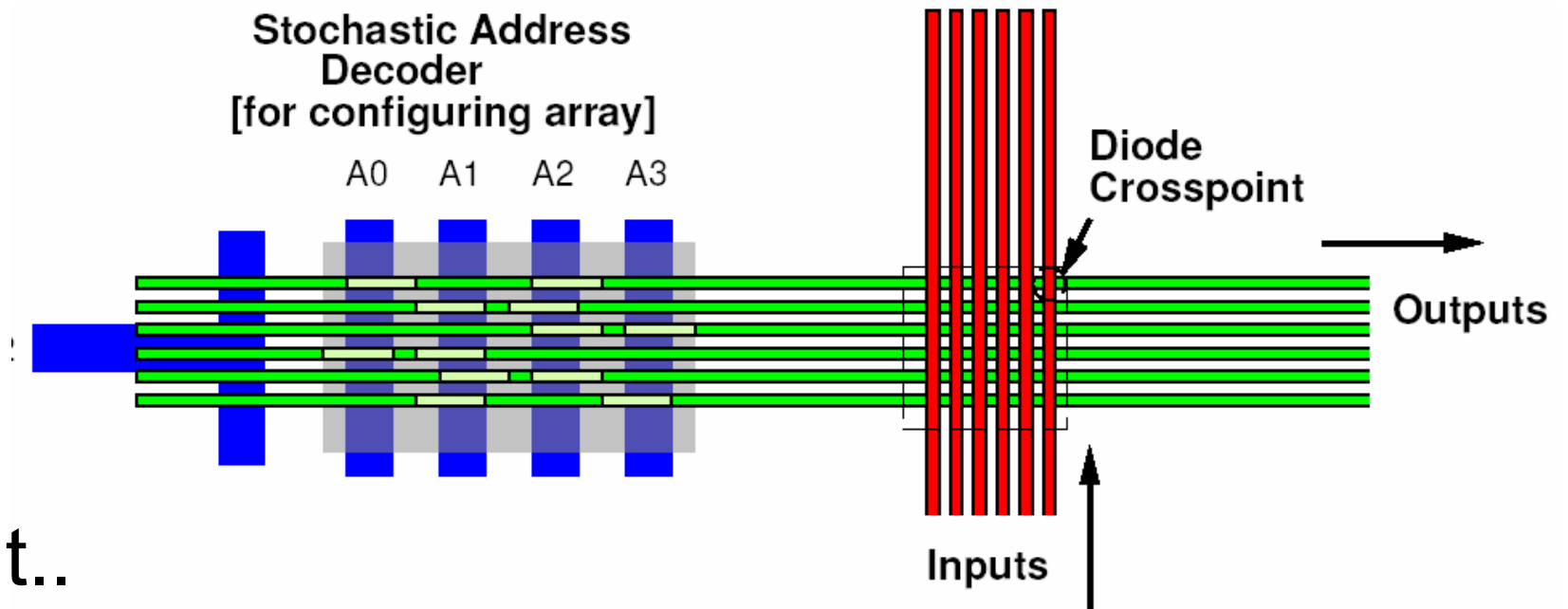
...on to Logic...

Diode Logic \rightarrow Wired OR

- Arise directly from touching NW/NTs
- Passive logic
- Non-restoring
- Non-volatile Programmable crosspoints



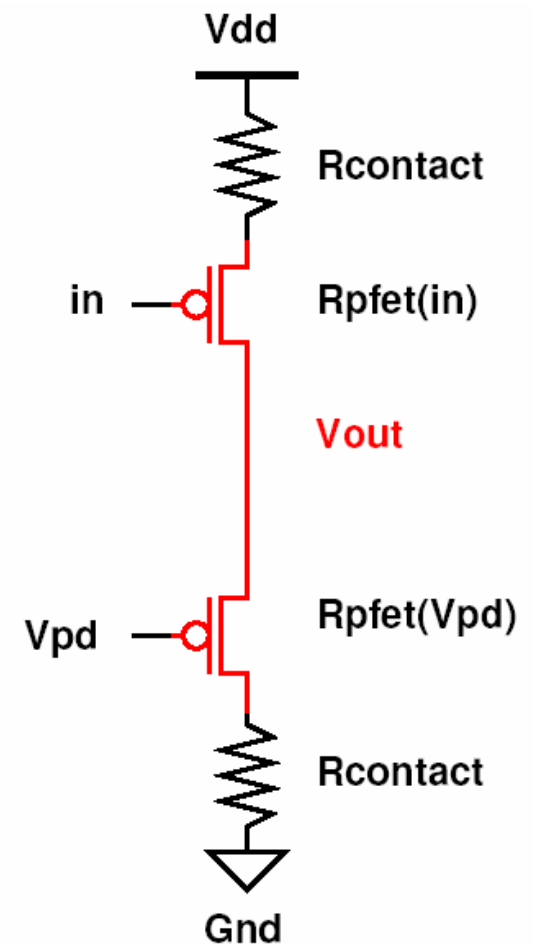
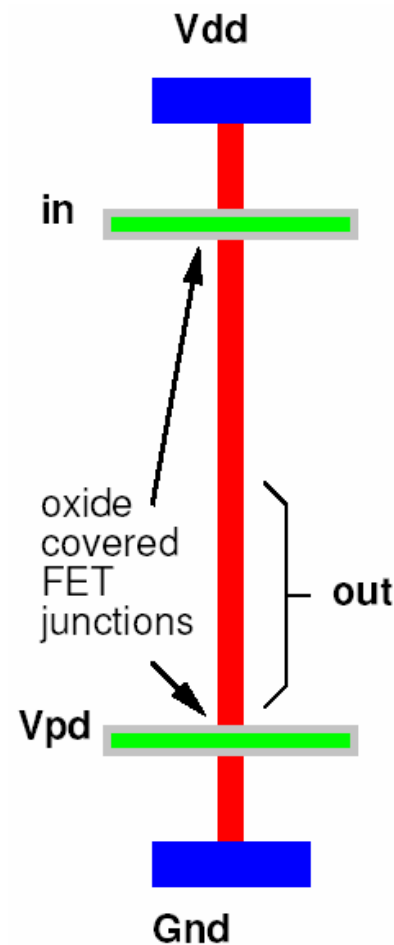
Use to build Programmable OR-plane



- But..
 - OR is not universal
 - Diode logic is non-restoring → no gain, cannot cascade

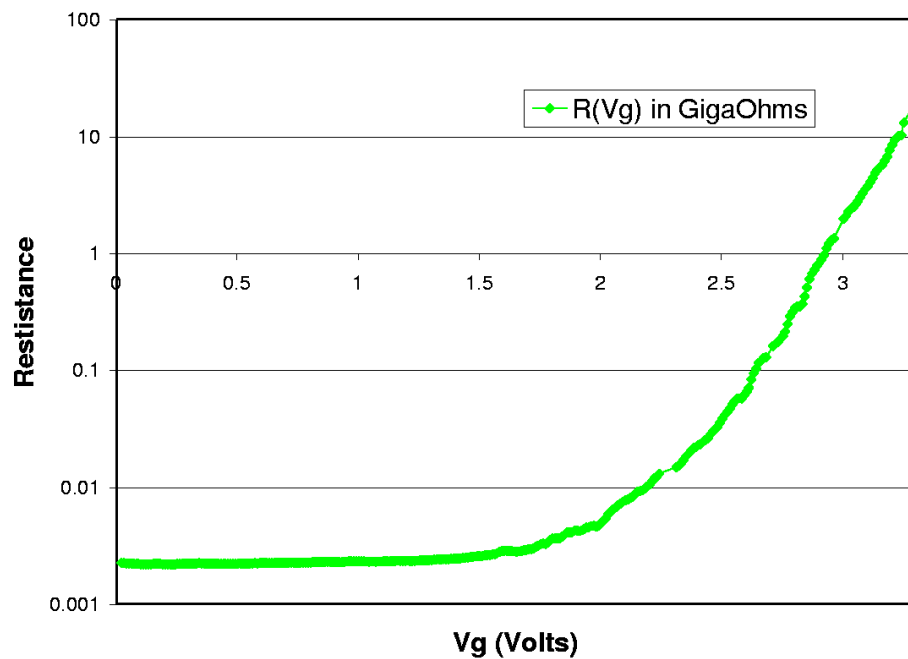
PMOS-like Restoring FET Logic

- Use FET connections to build **restoring** gates
- Static load
 - Like NMOS (PMOS)
- Maybe precharge



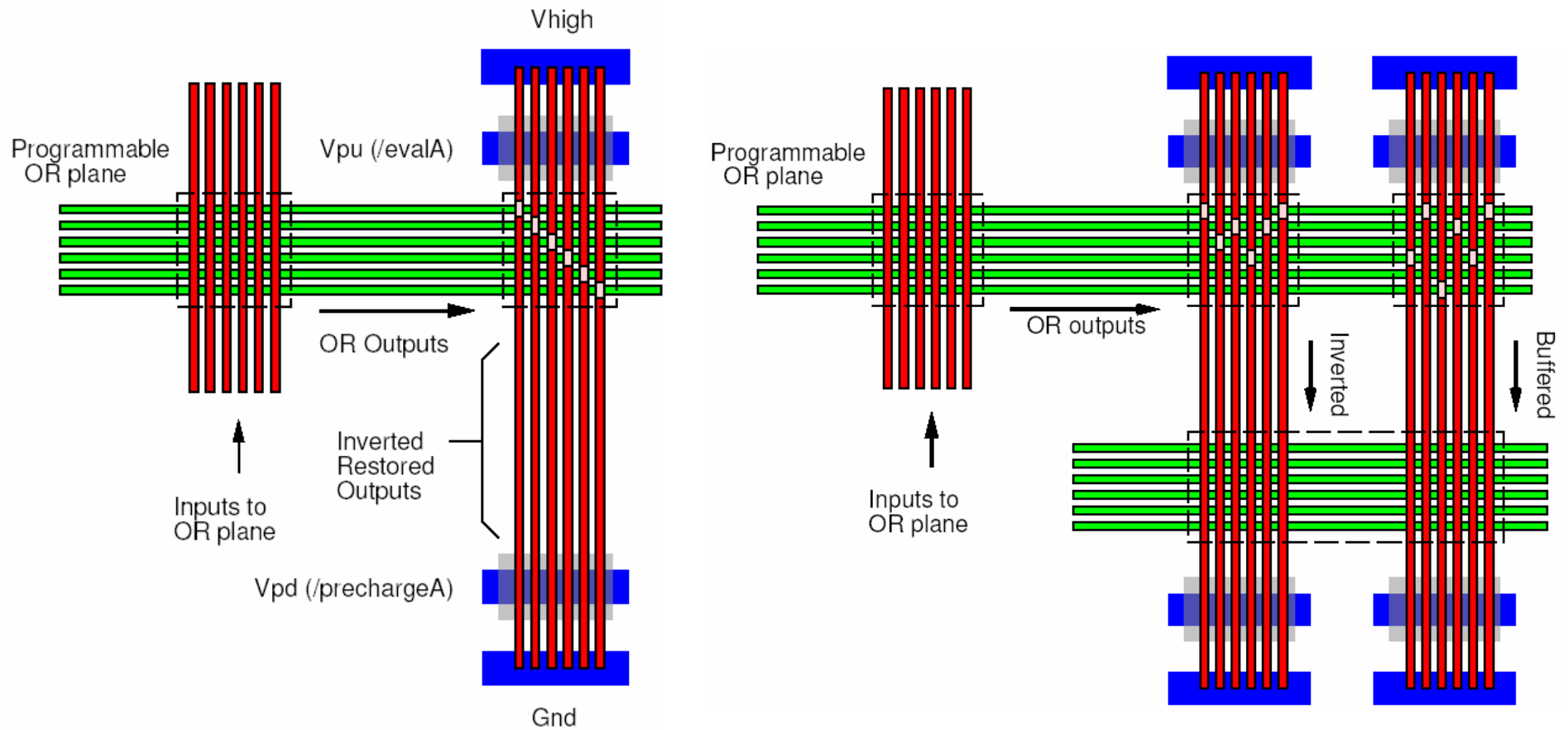
Operating Point: Make Restoring

$$V_{out} = V_{dd} \left(\frac{R_{pd} + R_c}{R_c + \sum_{i=0}^{M-1} (R_{pfet}(V_i)) + R_{pd} + R_c} \right)$$

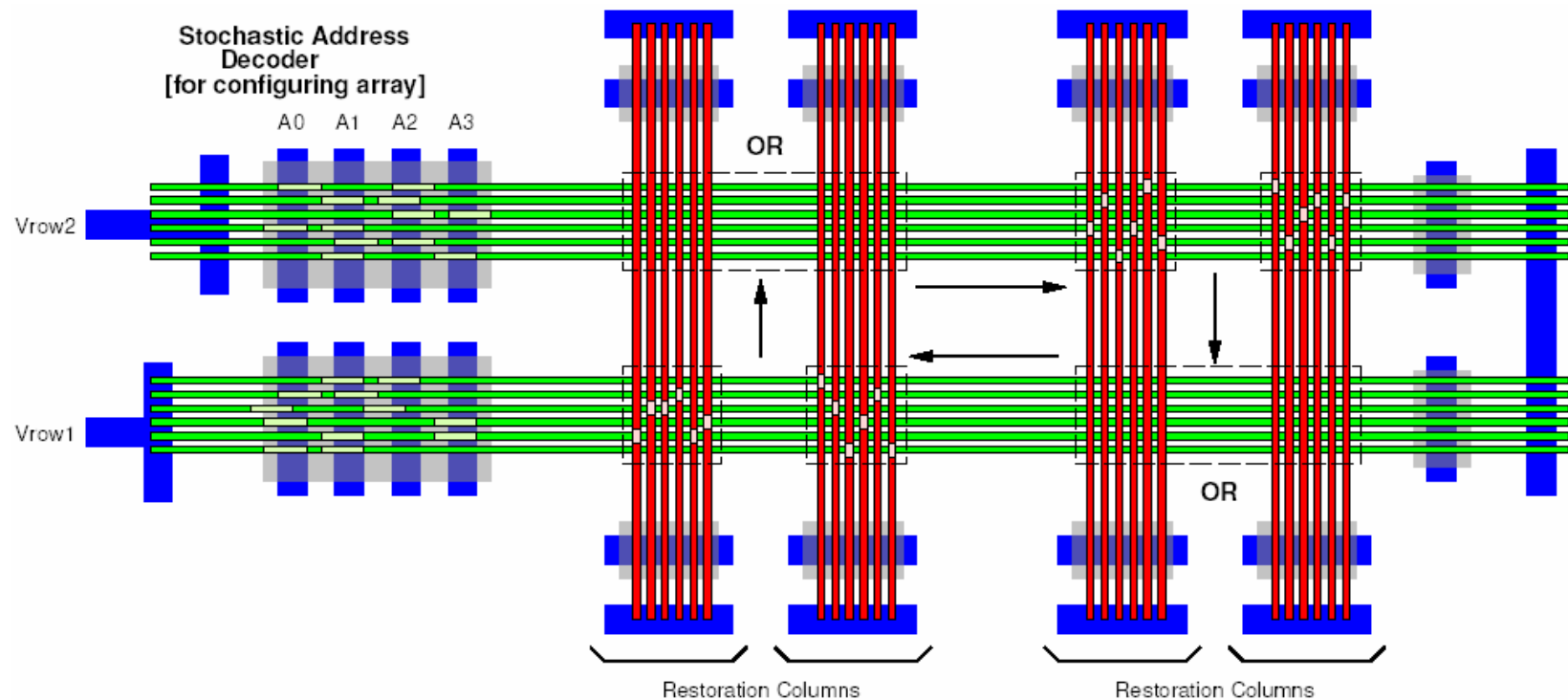


V_{dd}	3.3V
V_{oh}	3.0V
V_{ih}	2.8V
V_{il}	0.5V
V_{ol}	0.15V
V_{pd}	2.4V

Restoration Array



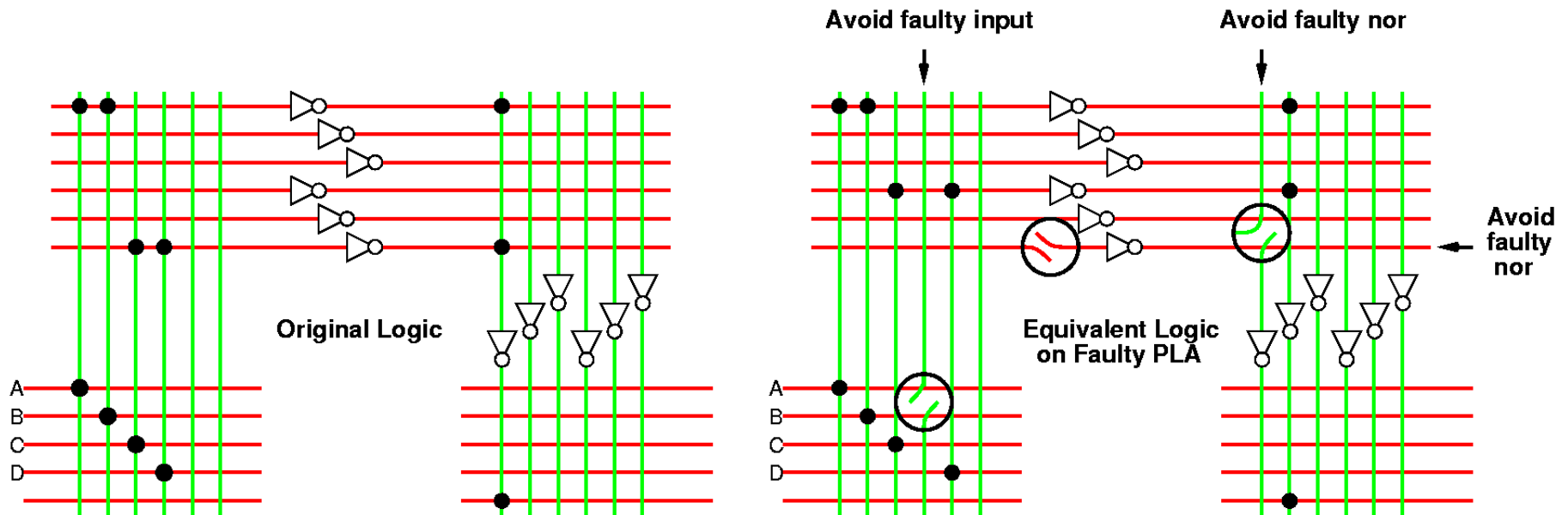
Simple Nanowire-Based PLA



NOR-NOR = AND-OR PLA Logic

FPGA 2004

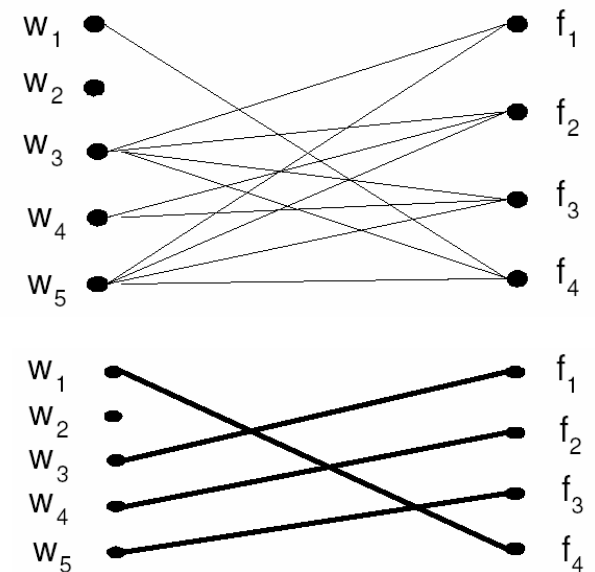
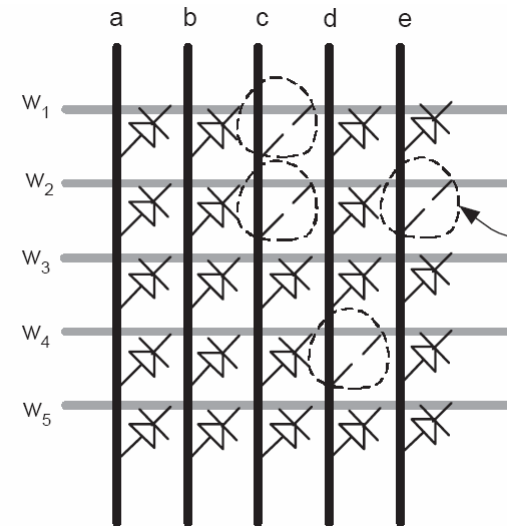
Defect Tolerant



All components (PLA, routing, memory) interchangeable;
Have M-choose-N property
Allows local programming around faults

Crosspoint Defects

- Crosspoint junctions may be nonprogrammable
 - *E.g.* HPs first 8x8 had 85% programmable crosspoints
- Tolerate by **matching** nanowire junction programmability with pterm needs
 - 10% \rightarrow <3x area of defect free

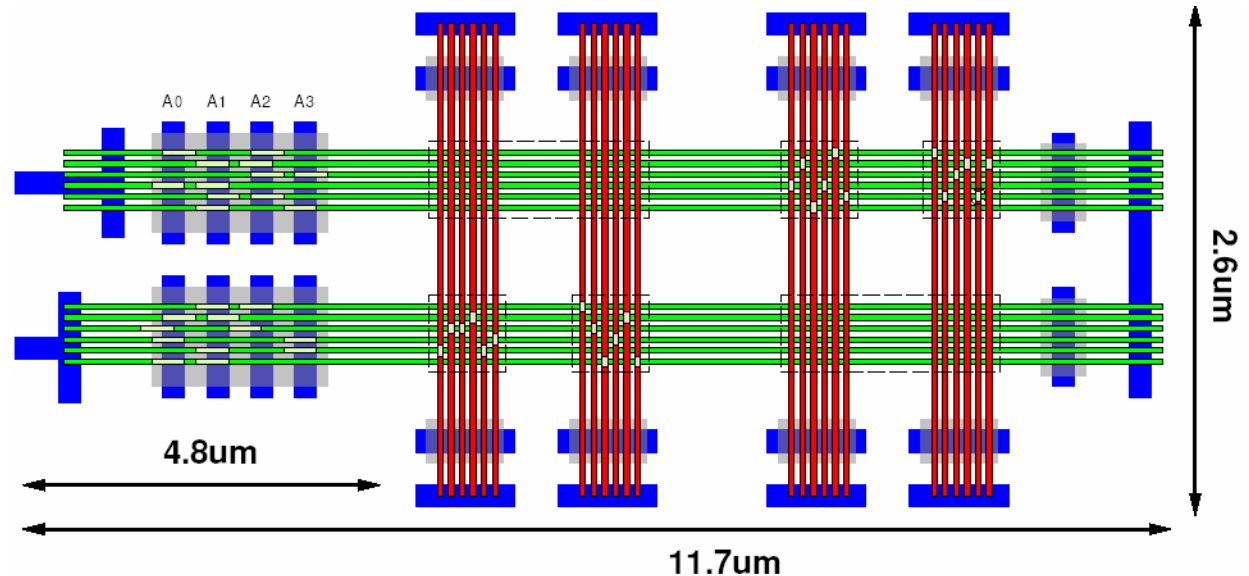


Naeimi/DeHon, FPT2004

Design and Test of Computers, July-August 2005

Simple PLA Area

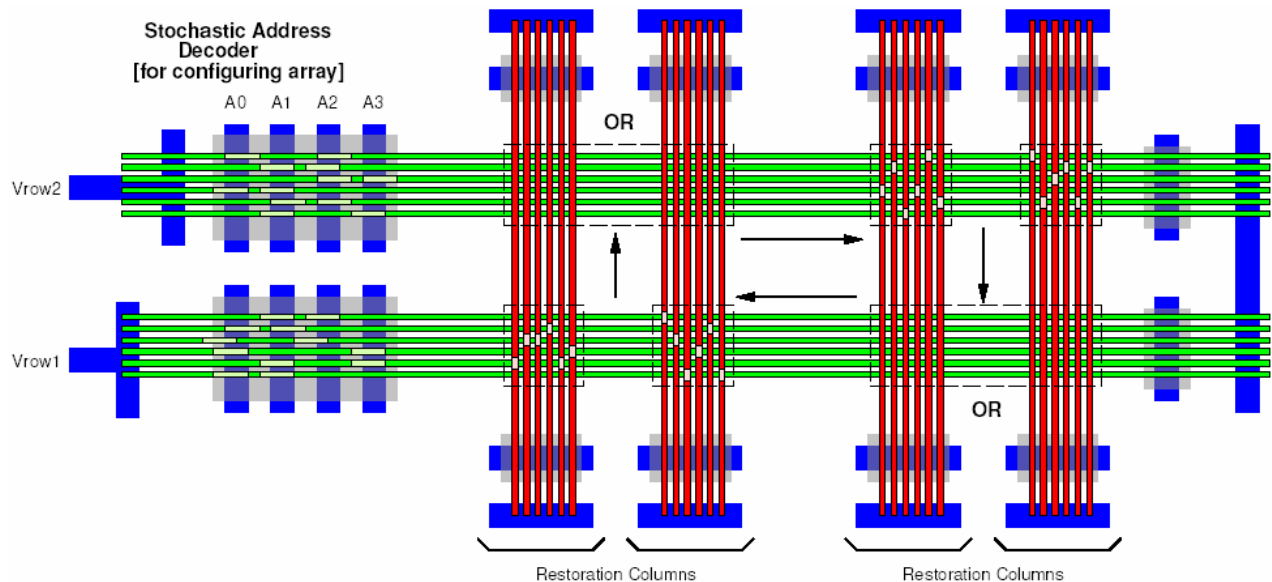
- 60 OR-term PLA
 - Useable
- 131 raw row wires
 - Defects
 - Misalign
- 171 raw inverting wires
 - Defects
 - Statistical population
- 60M sq. nm.
 - (2 planes)



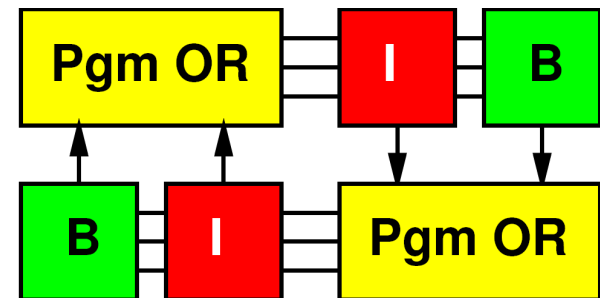
90nm support lithography;
10nm nanowire pitch

Scaling Up

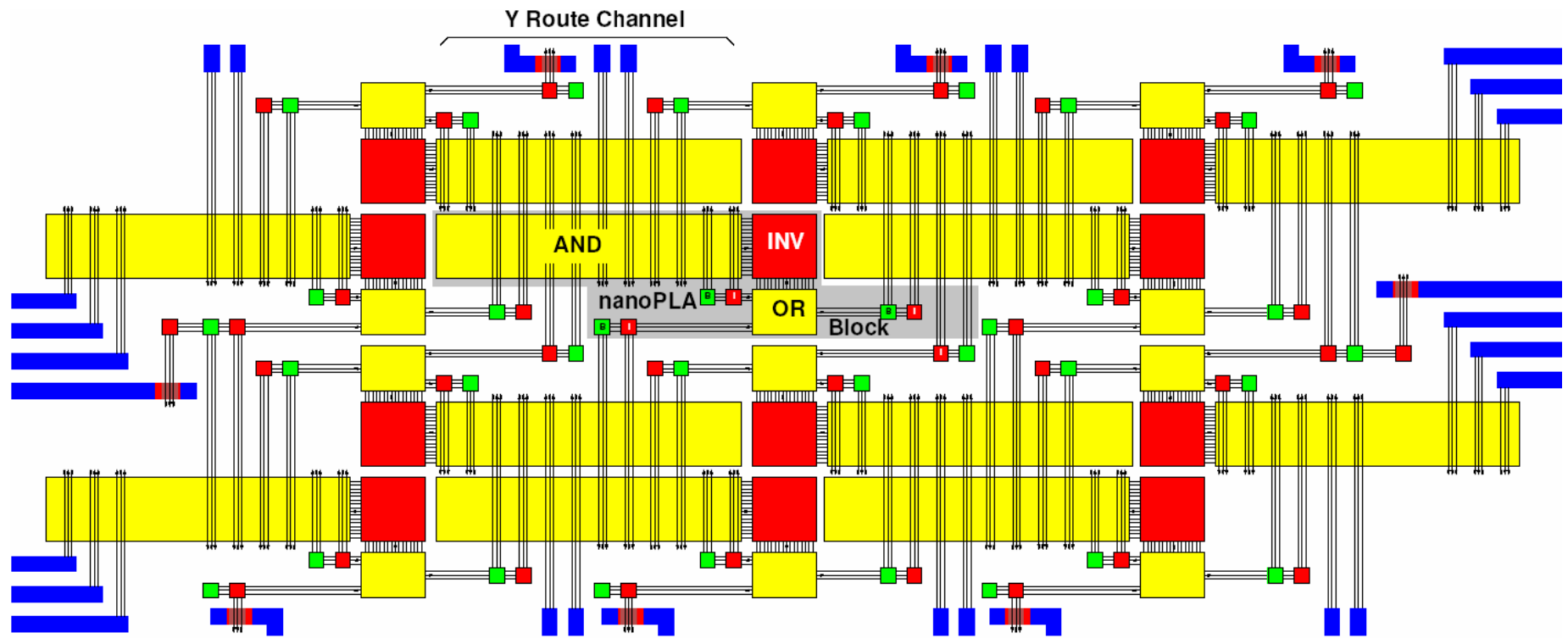
Scaling Up



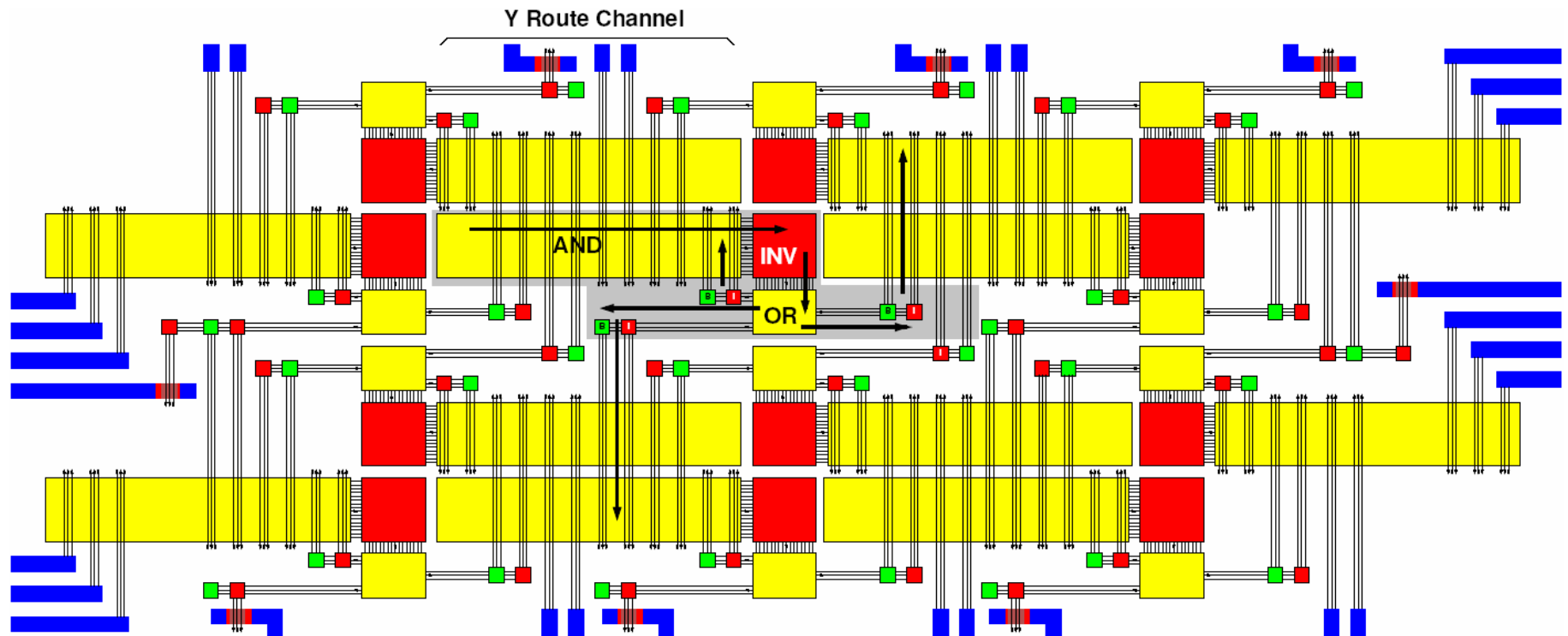
- Large arrays are not viable
 - Not exploit structure of logic
 - Long Nanowires tend to break
 - Long Nanowires will be slow



Interconnect nanoPLA Arrays

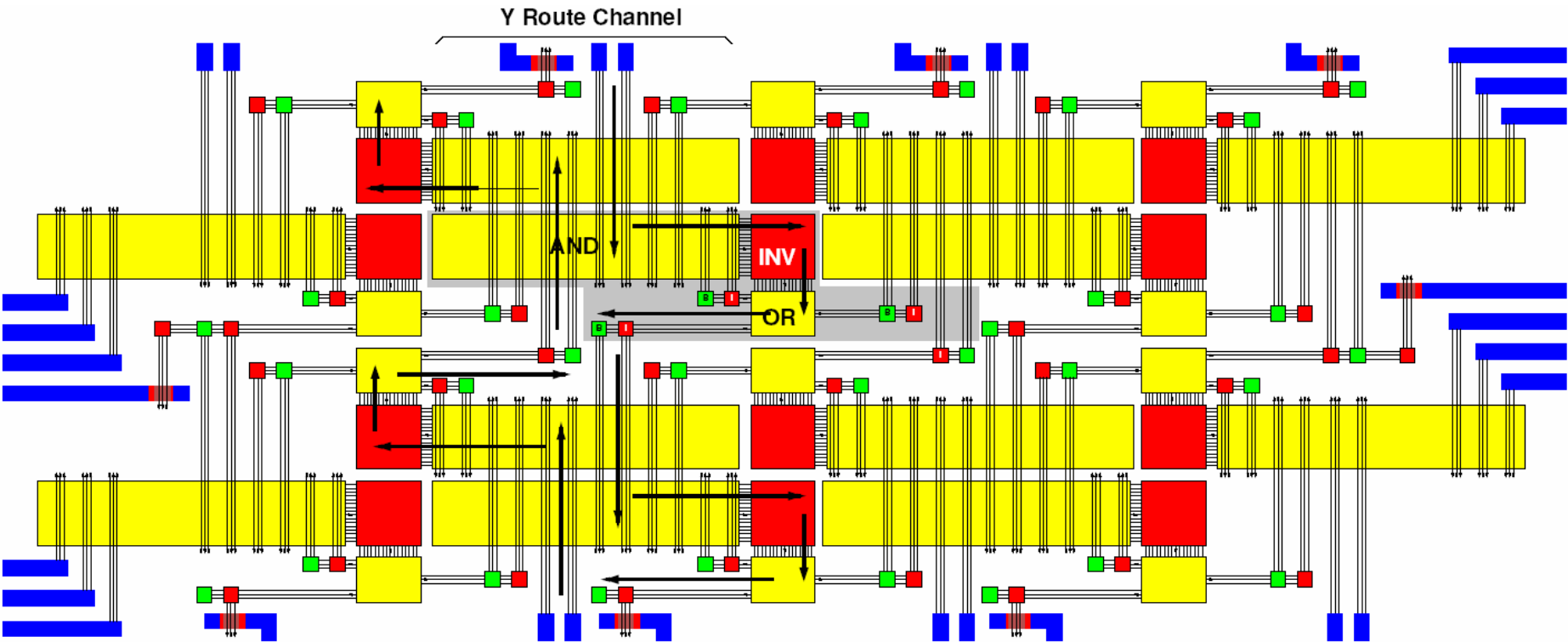


Interconnect nanoPLA Arrays

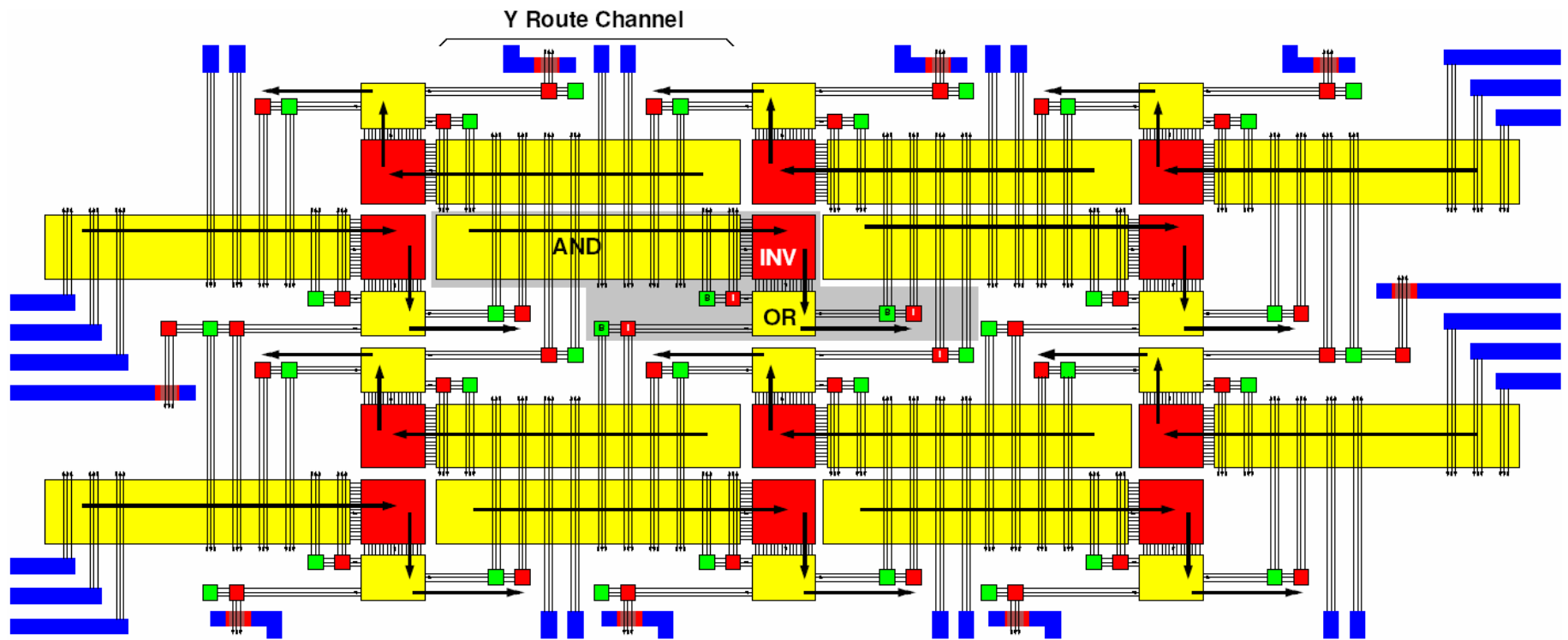


FPGA 2005

Interconnected nanoPLA Arrays

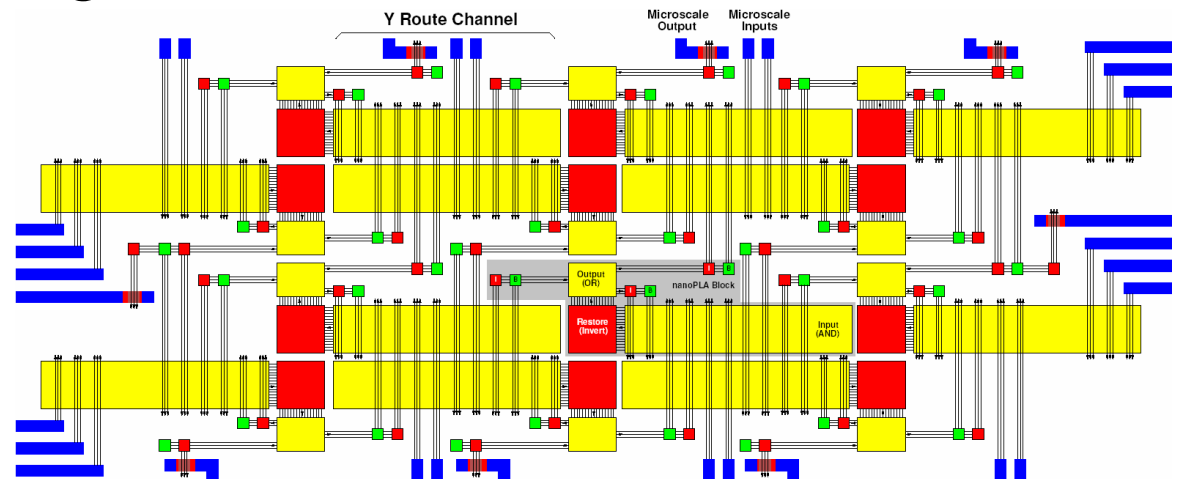


Interconnected nanoPLA Arrays

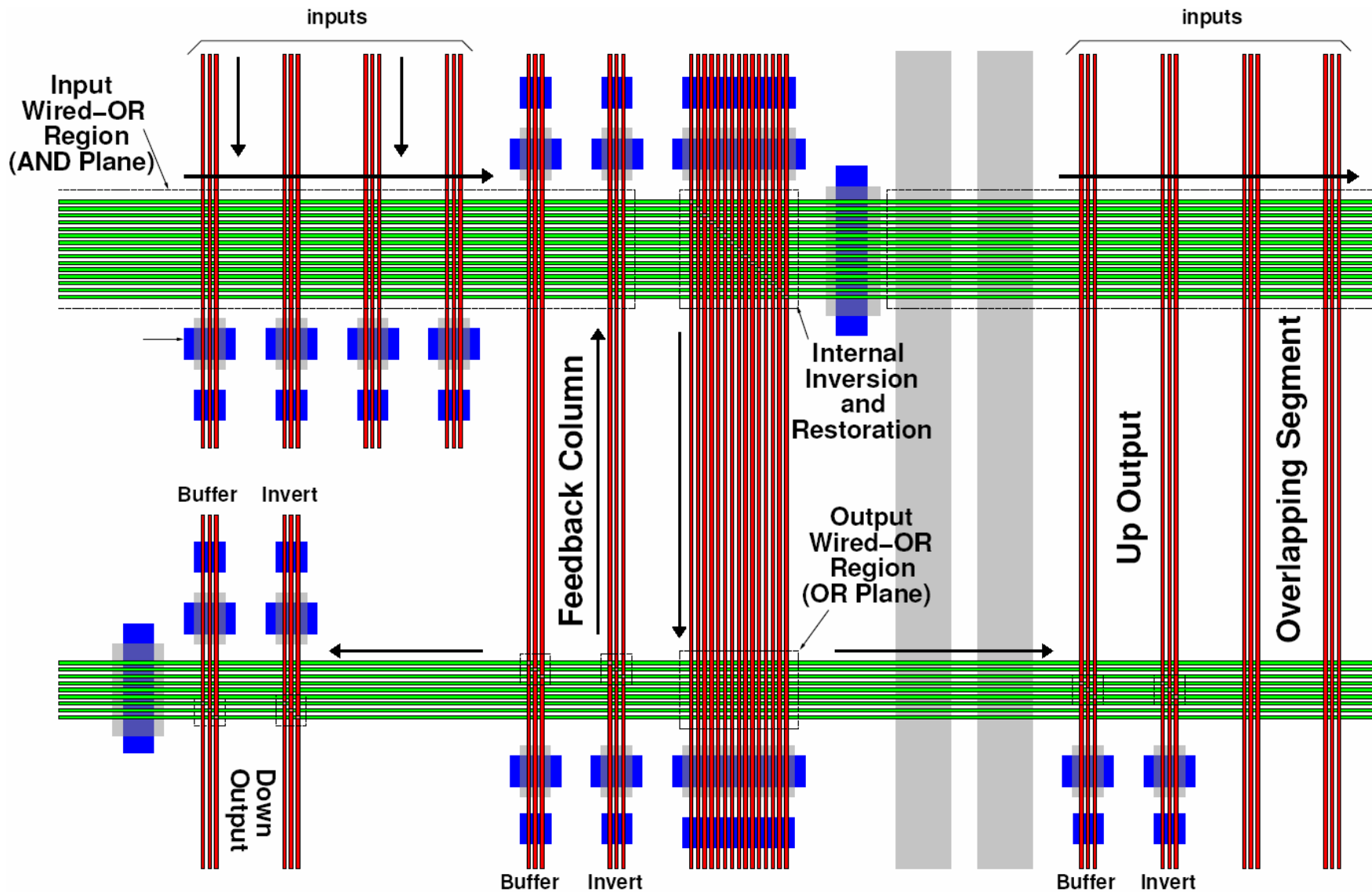
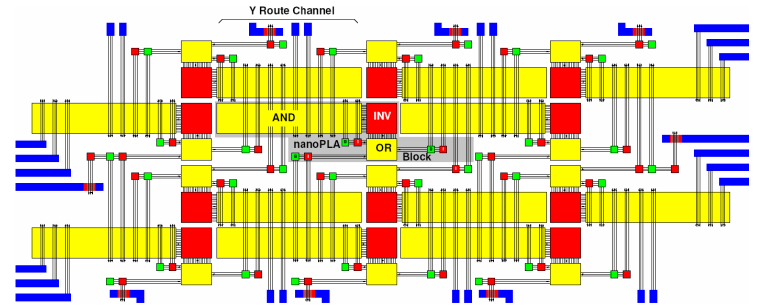


Complete Substrate for Computing

- Know NOR gates are universal
 - Selective inversion
 - Interconnect structure for arbitrary routing
 - Programmable structure similar to today's FPGAs
- Can compute any logic function
- Can combine with nanomemories



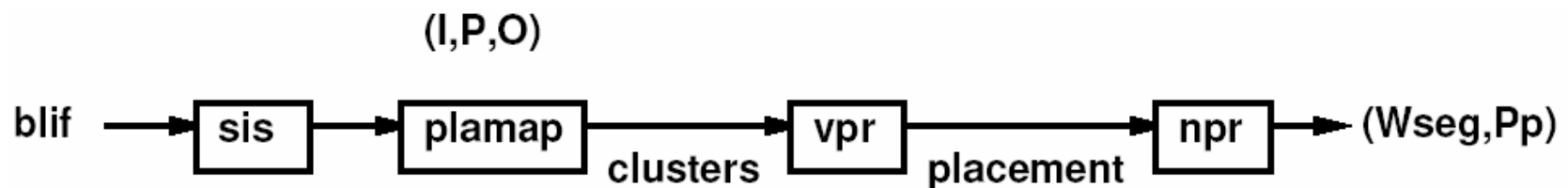
Interconnected nanoPLA Tile



Analysis

Area Mapped Logic

- Take standard CAD/Benchmark designs
 - Toronto20 used for FPGA evaluation
- Map to PLAs
- Place and Route on arrays of various configurations
- Pick Best mapping to minimize Area



Mapped Logic Density (105/10/5)

Design	Physical Params		4-LUTs	22nm CMOS ($\times 10^{11} \text{nm}^2$)	45 nm nanoPLA		
	P_p	W_{seg}			array org.	Area ($\times 10^8 \text{nm}^2$)	Area Ratio
alu4	60	8	1522	1.52	5×5	2.8	547
apex2	54	15	1878	1.88	14×14	28.3	66
apex4	62	7	1262	1.26	6×6	3.9	325
bigkey	44	13	1707	1.71	11×11	15.1	112
clma	104	28	8382	8.38	23×23	161.6	51
des	78	25	1591	1.59	12×12	35.2	45
diffeq	86	21	1497	1.50	11×11	27.1	55
dsip	58	18	1370	1.37	9×9	13.5	101
elliptic	78	27	3604	3.60	17×17	74.8	48
ex1010	66	9	4598	4.60	9×9	9.8	468
ex5p	67	18	1064	1.06	3×3	1.6	668
frisc	92	34	3556	3.56	18×18	110.8	32
misex3	64	8	1397	1.40	7×7	5.6	249
pdc	74	13	4575	4.58	7×7	7.5	610
s298	79	15	1931	1.93	8×8	11.0	176
s38417	76	22	6406	6.41	23×23	115.5	55
seq	72	18	1750	1.75	9×9	14.9	117
spla	68	12	3690	3.69	5×5	3.6	1025
tseng	78	25	1047	1.05	11×11	29.6	35

nanoPLA Mapped Logic Area

Defect Free
CMOS
 $F_{\text{cmos}} = 22\text{nm}$
4-LUT FPGA

VS

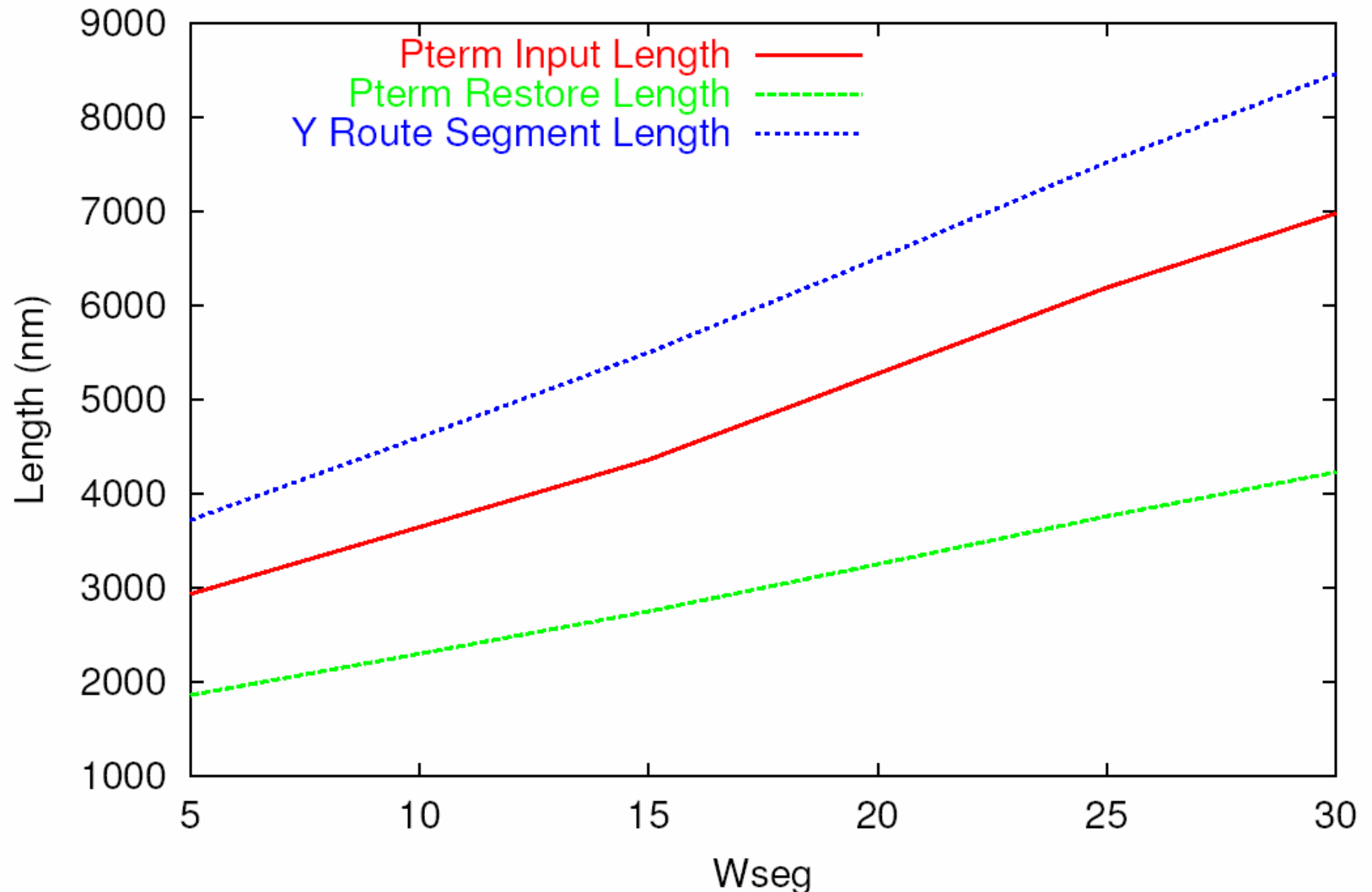
nanoPLA
 $F_{\text{cmos}} = 45$
 $F_{\text{nano}} = 5$

Design	Ratio	Design	Ratio
alu4	340	ex5p	390
apex2	39	frisc	17
apex4	200	misex3	150
bigkey	69	pdcc	360
clma	30	s298	105
des	26	s38417	32
diffeq	32	seq	69
dsip	59	spla	630
elliptic	27	tseng	20
ex1010	290		

Details see:
[JETC2005 v1n2p109](#)

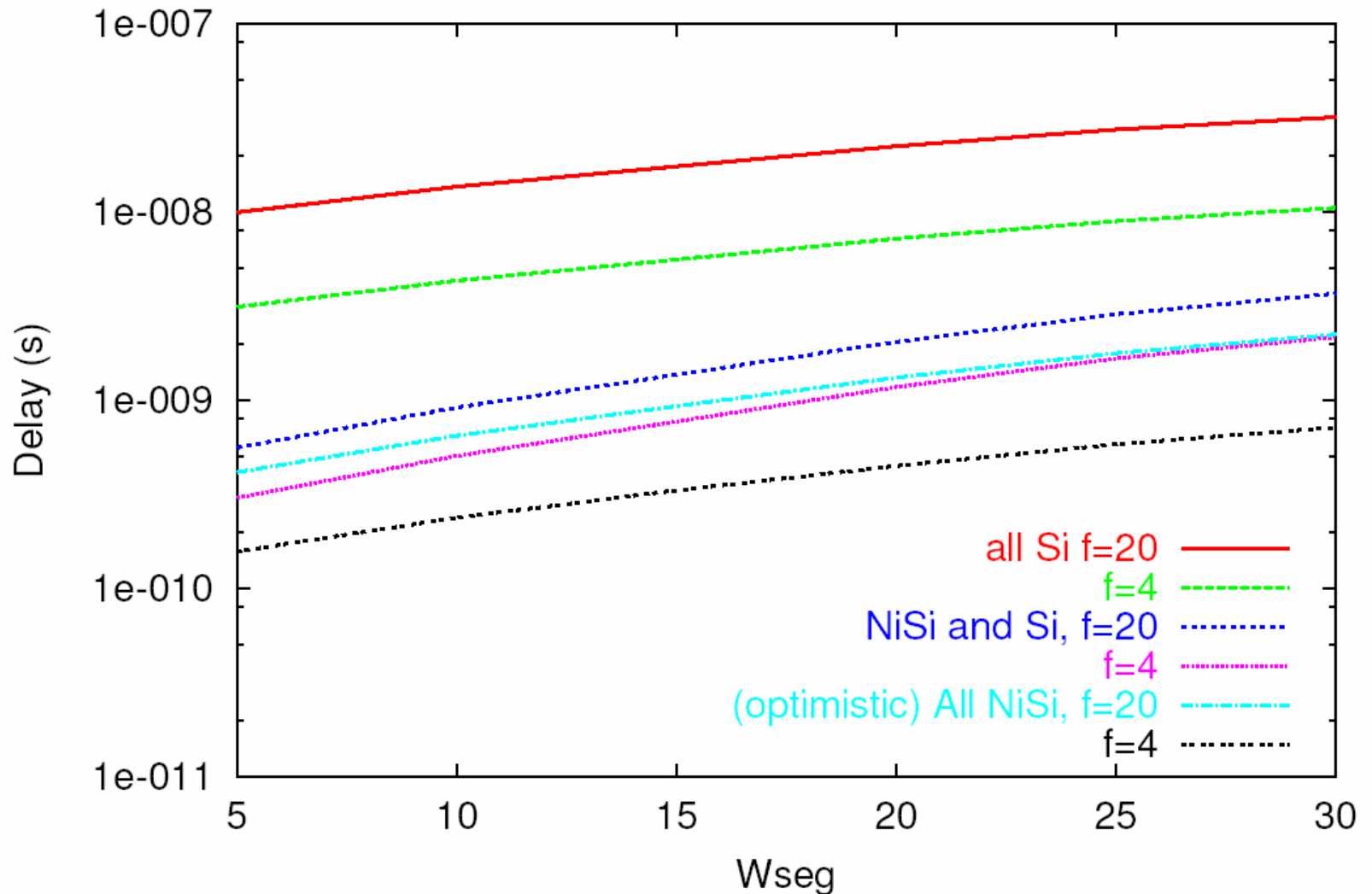
Nanowire Lengths: 105/10/5/Ideal Restore/ $P_c=0.95$

Wire Lengths vs. Wseg @ $P_{term}=4.0$



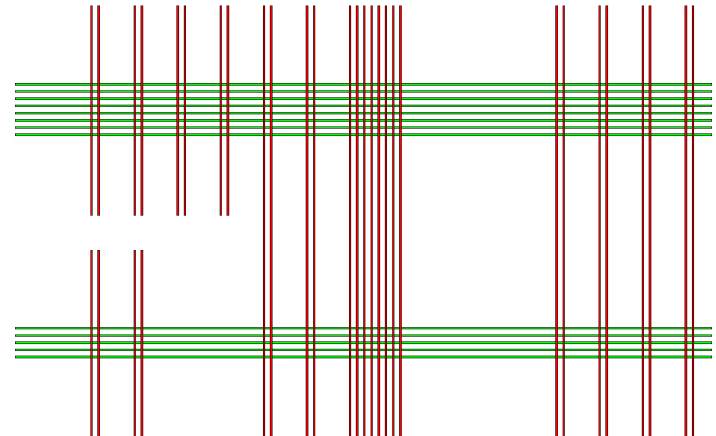
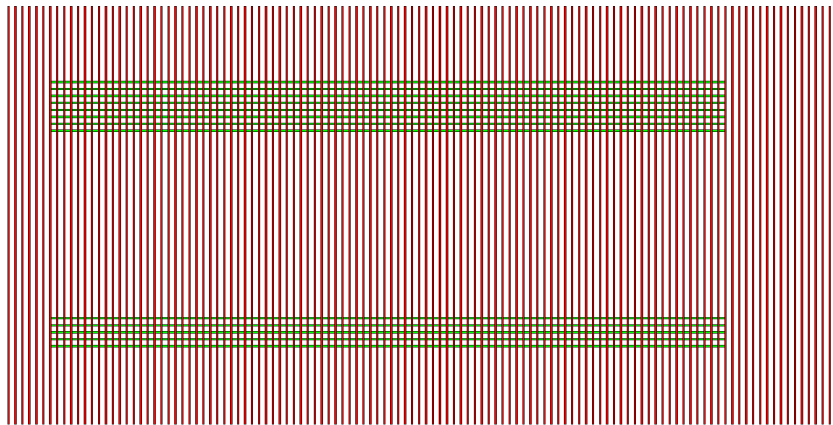
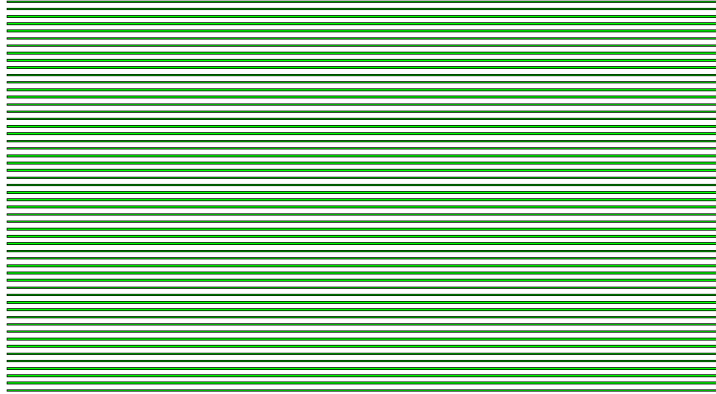
Cycle Delay: 105/10/5/Ideal Restore/ $P_c=0.95$

Delay vs. Wseg @ $P_{term}=4.0$

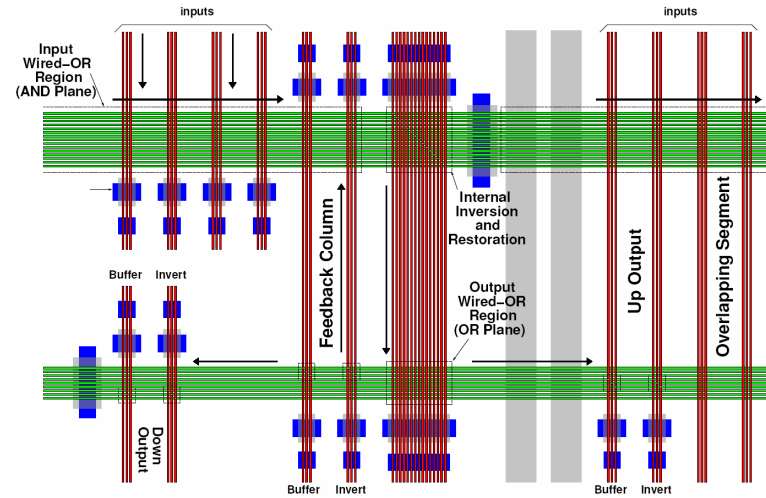
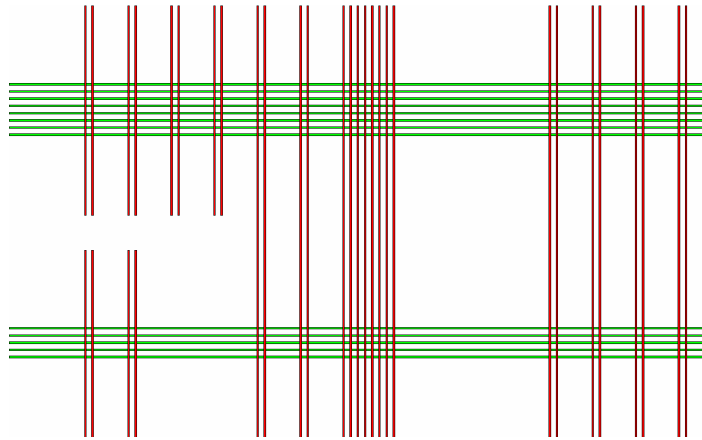


Construction

Manufacturing Flow



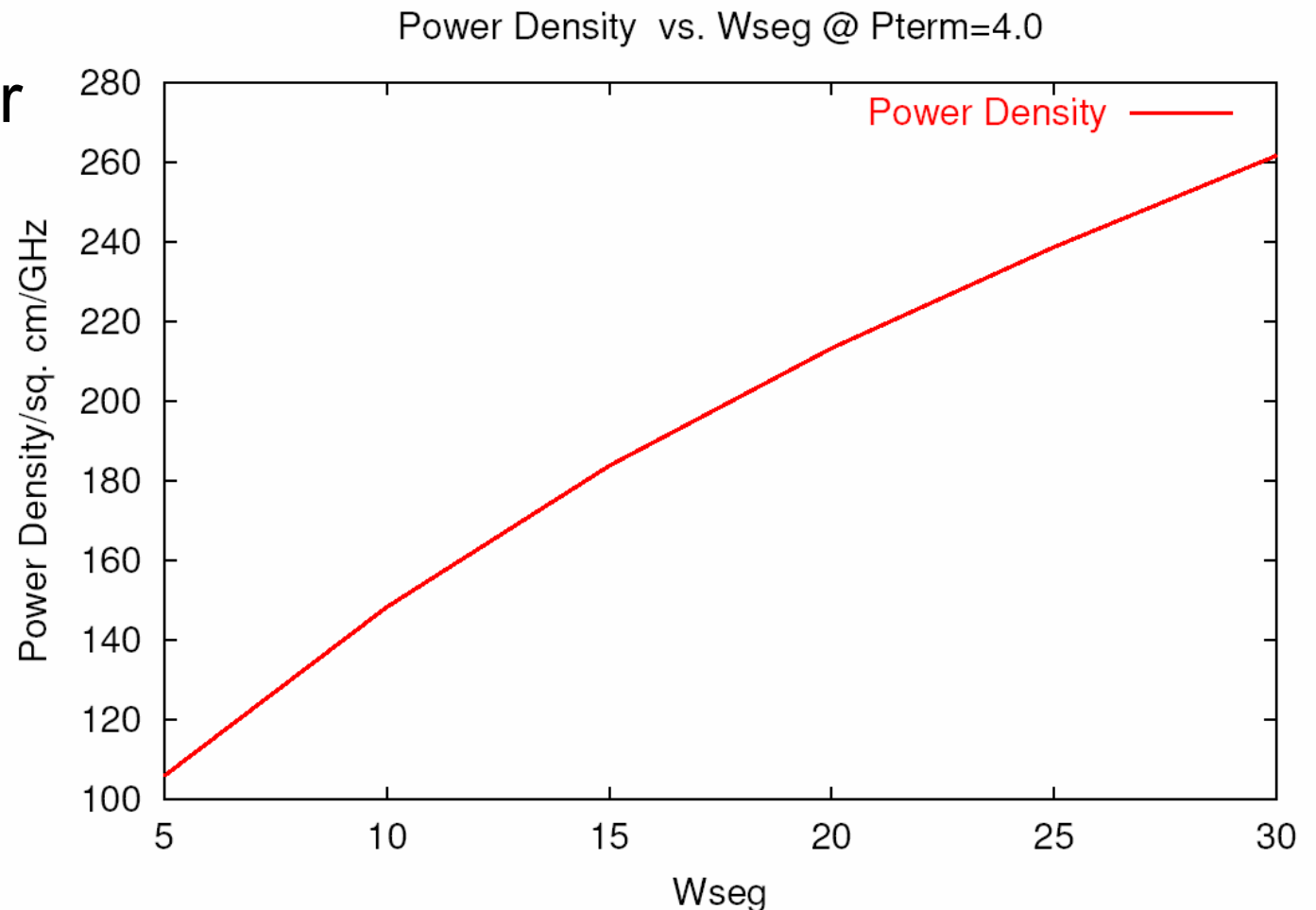
Manufacturing Flow

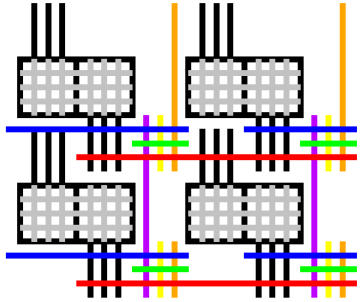


- Stochastic differentiation of Nanowires
- Post-fabrication configuration to define function and avoid defects

Power Density (per GHz)

- Vdd=1V
- Active Power
- Precharge





Summary

- Can engineer designer structures at atomic scale without lithographic patterning
- Must build regular structure
 - Amenable to self-assembly
- Can differentiate
 - Stochastically
 - Post-fabrication programming
- Sufficient building blocks to define universal computing systems
- Reach or exceed extreme DSM lithography densities
 - With modest lithographic support



Additional Information

- <<http://www.cs.caltech.edu/research/ic/>>
- <<http://www.cmliris.harvard.edu/>>

